SIERRA'S ANALOG-DIGITAL SIMULATOR SPEEDS ASIC DESIGN/60

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Electronics®

A NEW, EASY WAY TO DESIGN ASICs

PAGE 53

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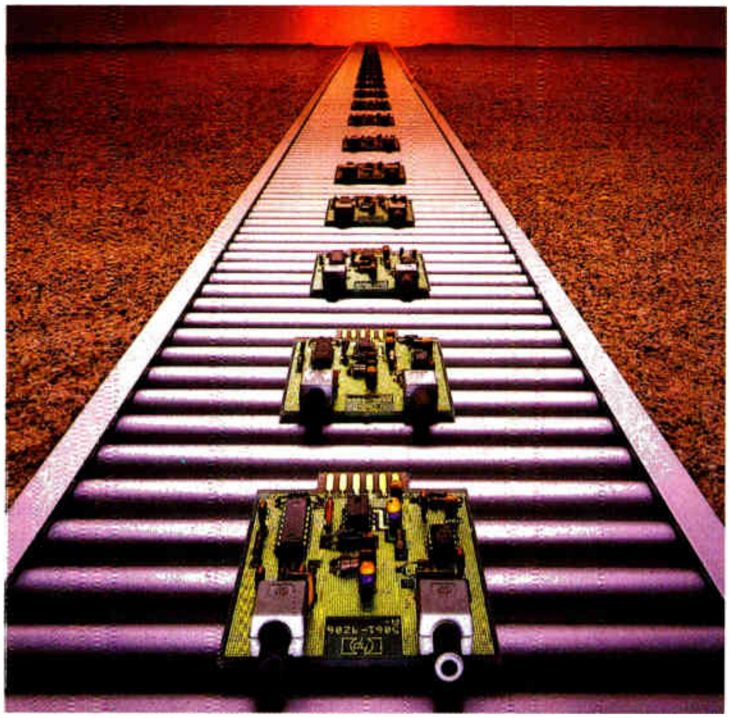
ELECTRONICS' ANNUAL TECHNOLOGY OUTLOOK

PAGE 67

Circle 900 on reader service card

SURPRISE!

Low-cost fiber-optic components for high-volume manufacturing.



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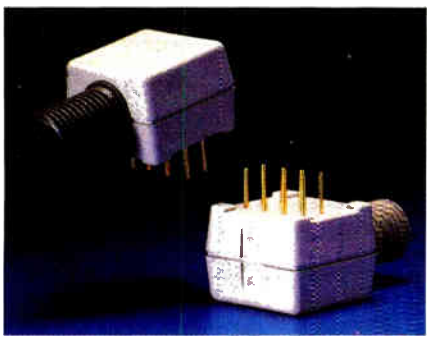

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Back on Oct. 17, 1974, we published a special technology update issue and wrote, "We plan to do it annually." We've been true to our word; the 13th edition of the much-imitated yearly roundup of the industry's best starts on page 67.

But the emphasis of these yearly reports has been moving more and more toward the future, adding the value you've come to expect from *Electronics*, the extra mile that our competitors simply cannot stretch. So with this year's report we are recognizing in name what has long been a deed: from now on, what was once Technology Update is now Technology Outlook.

Sam Weber, executive technical editor, has shepherded these reviews into print every year since their inception. He recalls well how the project got rolling. "The genesis of the annual update was a special issue we had done the previous year—on Oct. 25, 1973, to be exact," he says. "We saw that electronics was making a move to take over many mechanical functions, such as watches and calculators, so we conceived a special issue reviewing the overall progress and growing pervasiveness of the technology we cover. It was called The Great Takeover, and it was so successful that we decided to do it annually as an update of the innovations in technology."

Since that first one, the idea of doing some sort of annual roundup has been copied by many other publications covering the electronics industry. However, "they may think they're copying it," says Sam. "Anyone can sit down with the articles that appeared in the past year and write a review from them. But only *Electronics* has the staff in cities around the world to lend a global perspective to the technology. And now we are giving our readers even more of that perspective on a look into the future."

WEBER: "Only *Electronics* has the staff to lend a global perspective to the technology."

Not to be outdone in the added-perspective department is our news staff, which is responsible for the profiles of leading lights in each field that are part of the Technology Outlook. There are seven this year, and one is doing a curtain call: B. J. Moore, who developed the first logic timing analyzer, the Biomation 810-D, was a co-winner of the 1977 Electronics Achievement Award. For what he is up to now, see Cliff Barney's profile on page 99.

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Electronics

NEWS

INSIDE TECHNOLOGY

PROBING THE NEWS

COVER: DORON BEN-AMI

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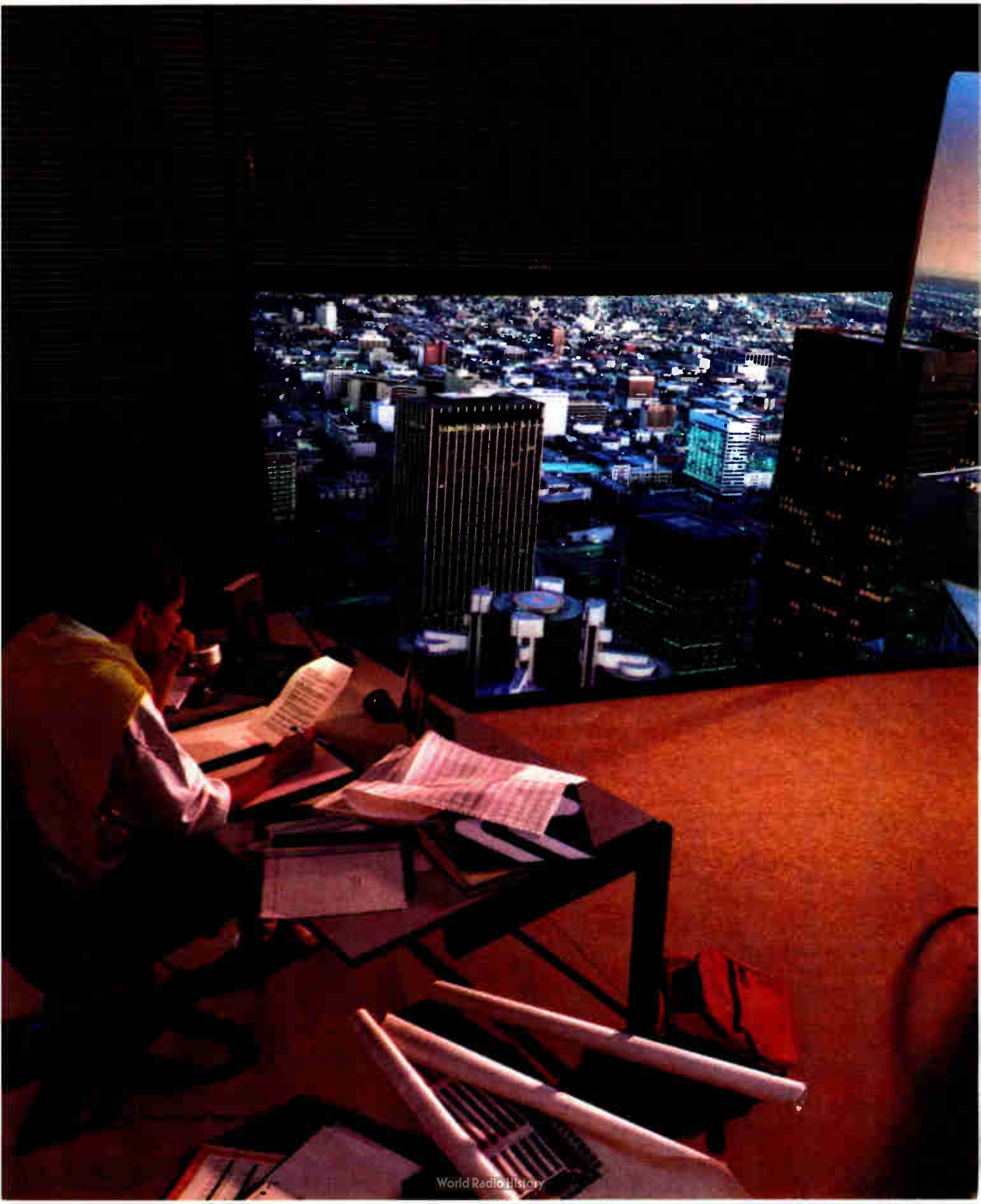
NEW PRODUCTS

DEPARTMENTS



Xerox spent a year examining the same ASIC companies you're looking at now.

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FYI

There seems to be no doubt that Fairchild is back; the big problem now is for its management to keep the momentum going, even if its parent ends up selling the store

For Fairchild Semiconductor, the Oct. 1 departure of Michel Vaillaud as chairman of its parent, Schlumberger Ltd., most likely came as a real shock. It certainly couldn't have come at a worse time. The nation's No. 6 chip maker has been making dramatic progress recently in positioning itself to grab market share when business turns up. And management at the Cupertino, Calif., company had regarded Vaillaud as a patient friend: he'd been willing to wait for Fairchild to move back solidly into the black.

The picture has suddenly changed under new chairman D. Euan Baird. Schlumberger is growing impatient. Wall Street expects the oilfield services company, which already has been slicing people and consolidating operations everywhere, to sell Fairchild, perhaps before the end of this year. But who would buy it? Chip makers are not regarded as the most exciting investment these days. And the price would not be cheap. In the past seven years Schlumberger has probably sunk more than $1.2 billion into its ailing subsidiary.

Maybe this is an opportunity for President Don Brooks and his band of Texas Instruments expatriates, who moved out West in the past few years. They clearly have made the difference at Fairchild. In February, *Electronics* reported on how ex-TIer Brooks was rejuvenating the venerable chip maker with a vigorous product-introduction program and a new strategy for survival. We outlined how he was trying to leapfrog his competition and emerge as a leading supplier of high-performance components for the next generation of computer systems. To build his technology base, Brooks had spent more than $135 million in 1985 on capital improvements.

"We're getting into fine shape for the upturn," declared a Fairchild manager last week. He figures the company is in the best situation that it's been in many years from a technology, product, and management standpoint. "We're now positioned very well in logic," this manager claims. "In fact we're in a good position to double our sales in the next two to three years." That would mean annual sales of more than $1 billion.

Without a doubt, Schlumberger has left Brooks and his team alone, and it is paying off. Today there seems to be no doubt that Fairchild is back. The big problem now for Brooks is to keep the momentum going, even if Fairchild's parent ends up selling the store. **ROBERT W. HENKEL**

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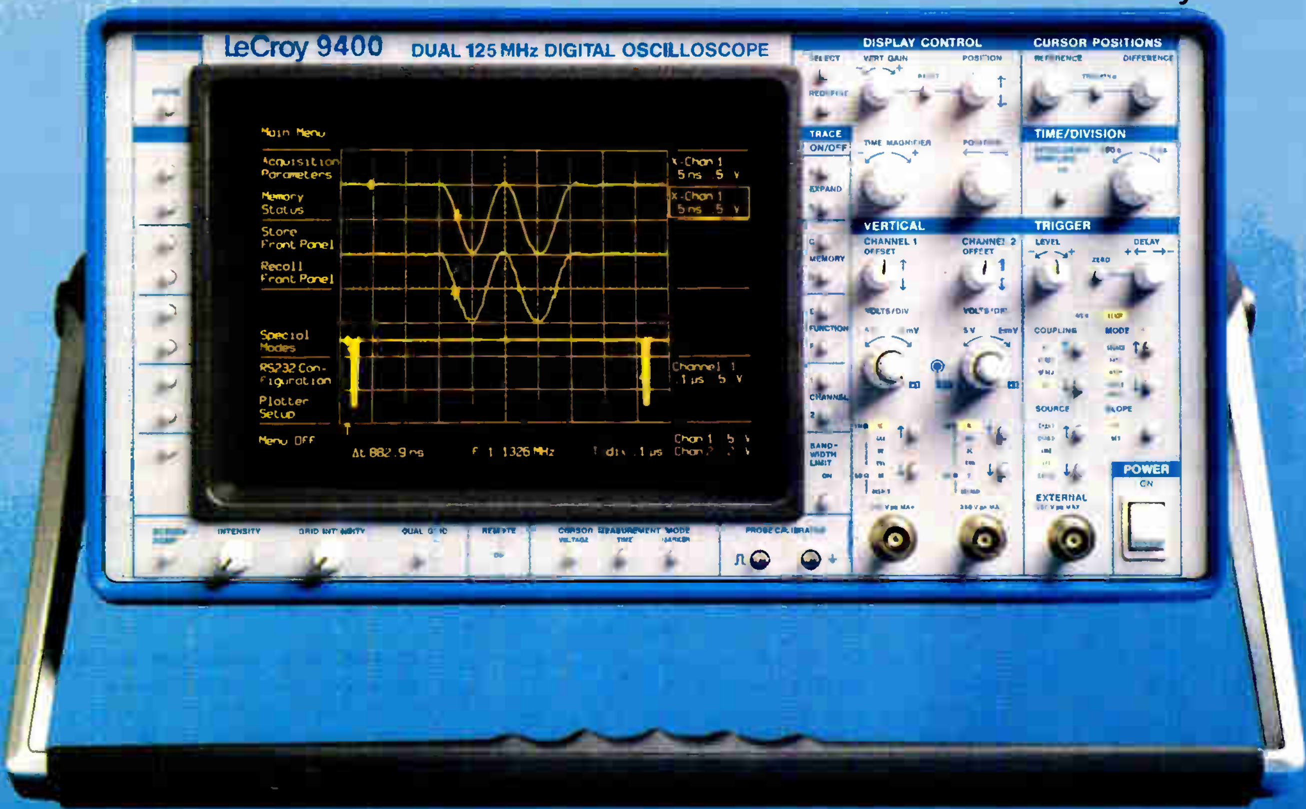

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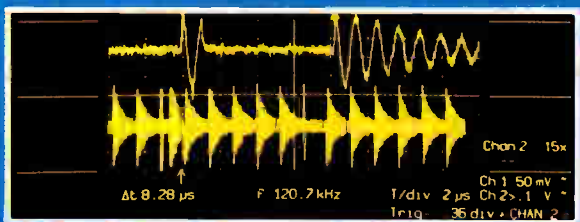

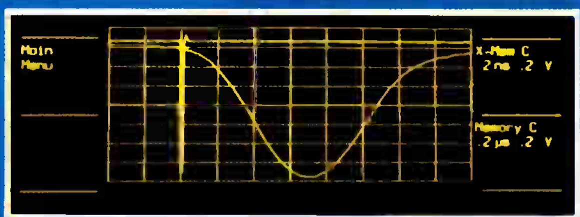

Top. Dual Zoom and time cursors are applied to measure delay between double pulses with 100 ps resolution and 0.002% precision.

Middle: Channel 2 is segmented in 15 partitions of 2,000 words each. Expansion of event 3 appears on top.

Below: A 10 ns wide pulse is digitized with 5 GS/s interleaved sampling speed. Expansion to 2 ns/div shows outstanding time and screen resolution.

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MEETINGS

International Congress on Applications of Lasers and Electro-Optics, Laser Institute of America, *et al.* (5151 Monroe St., Suite 102W, Toledo, Ohio 43623), Sheraton National Hotel, Arlington, Va., Nov. 10-13.

ICCAD '86, International Conference on Computer Aided Design, Computer Society of IEEE, *et al.* (1730 Massachusetts Ave., N.W., Washington, D.C. 20036), Santa Clara Convention Center, Santa Clara, Calif., Nov. 10-13.

COMDEX/Fall, The Interface Group Inc. (300 First Ave., Needham, Mass. 02194), Las Vegas Convention Center, Las Vegas, Nev., Nov. 10-14.

Winter National Design Engineering Conference, American Society of Mechanical Engineers (Cahners Exposition Group, 999 Summer St., P.O. Box 3833, Stamford, Conn. 06905), Moscone Center, San Francisco, Calif., Nov. 11-13.

Sensors '86, Society of Manufacturing Engineers (One SME Drive, P.O. Box 930, Dearborn, Mich. 48121), Westin Hotel, Dearborn, Mich., Nov. 11-13.

Autofact '86, Computer and Automated Systems Association of Society of Manufacturing Engineers (One SME Drive, P.O. Box 930, Dearborn, Mich. 48121), Cobo Hall, Detroit, Mich., Nov. 11-14.

DAK/DAP (CAD/CAM) '86, Norwegian Computer Society, *et al.* (Messebyraet As. Sandviksvn. 184, Postboks 530, N-1301 Sandvika), Info-Rama Centre, Sandvika, Norway, Nov. 11-14.

GOMAC '86: Government Microcircuit Applications Conference, Department of Defense, *et al.* (Palisades Institute for Research Services Inc., 201 Varick St., 11th Flr., New York, N. Y. 10014), Sheraton on Harbor Island–East, San Diego, Calif., Nov. 11-13.

Electronica '86 and 12th International Microelectronics Conference, Munich Fair and Expositions GmbH, *et al.* (Postfach 12 1009, D-8000 Munchen 12, West Germany), Munich Trade Fair Center, Munich, Nov. 11-15.

CADDM '86: International Conference on Computer-Aided Drafting, Design, and Manufacturing, Automation Technology Institute, *et al.* (P.O. Box 242, Pebble Beach, Calif. 93953), Beijing, China, Nov. 11-15.

International Workshop on Moisture, Measurement, and Control for Microelectronics, National Bureau of Standards, *et al.* (Dr. Didier Kane, Rome Air Development Ctr., Griffiss AFB, N.Y. 13441), NBS, Gaithersburg, Md., Nov. 12-14.

Fallcon '86, IEEE Cedar Rapids Section (P.O. Box 451, Marion, Iowa 52302), Stouffer's Five Seasons Hotel, Cedar Rapids, Iowa, Nov. 12-13.

India International Trade Fair, Republic of India (Commerce Counsellor, Indian Embassy, 2107 Massachusetts Ave., N.W., Washington, D.C. 20008), New Delhi, India, Nov. 14-30.

International Electronics Packaging Conference, International Electronics Packaging Society (114 N. Hale St., Suite 2B, Wheaton, Ill. 60187), Sheraton on Harbor Island–East, San Diego, Calif., Nov. 17-19.

Training Systems Conference, National Security Industrial Association (P. J. Cole, NSIA, 1015 15th St., N.W., Suite 901, Washington, D.C. 20005), Salt Palace, Salt Lake City, Utah, Nov. 17-20.

Conference on Magnetism and Magnetic Materials, American Institute of Physics, *et al.* (Diane S. Suiters, Courtesy Associates, 655 15th St., N.W., Suite 300, Washington, D.C. 20005), Hyatt Regency, Baltimore, Md., Nov. 17-20.

Scientific Software for Supercomputing, National Bureau of Standards (Francis Sullivan, A151 Technology Building, NBS, Gaithersburg, Md. 20899), NBS, Gaithersburg, Md., Nov. 17-20.

Plastics in Electronics, Business Communications Inc. (9 Viaduct Rd., Stamford, Conn. 06907), Crowne Plaza Holiday Inn, Stamford, Conn., Nov. 18-19.

Wescon '86, IEEE (Electronics Conventions Inc., 8110 Airport Blvd., Los Angeles, Calif. 94303), Convention Center, Anaheim, Calif., Nov. 18-21.

International Exhibition of Equipment and Products for Electronics, Société de Diffusion des Sciences et des Arts (20, rue Hamelin, F 75116 Paris, France), Porte de Versailles Exhibition, Paris, Nov. 18-21.

Microcontamination Conference and Exposition, Microcontamination Magazine (Expocon Management Associates Inc., 3695 Post Rd., Southport, Conn. 06490), Santa Clara, Calif., Nov. 18-21.

Power Electronics and Variable-Speed Drives '86, Institution of Electrical Engineers (Savoy Place, London WC2R 0BL, U.K.), National Exhibition Centre, Birmingham, England, Nov. 25-27.

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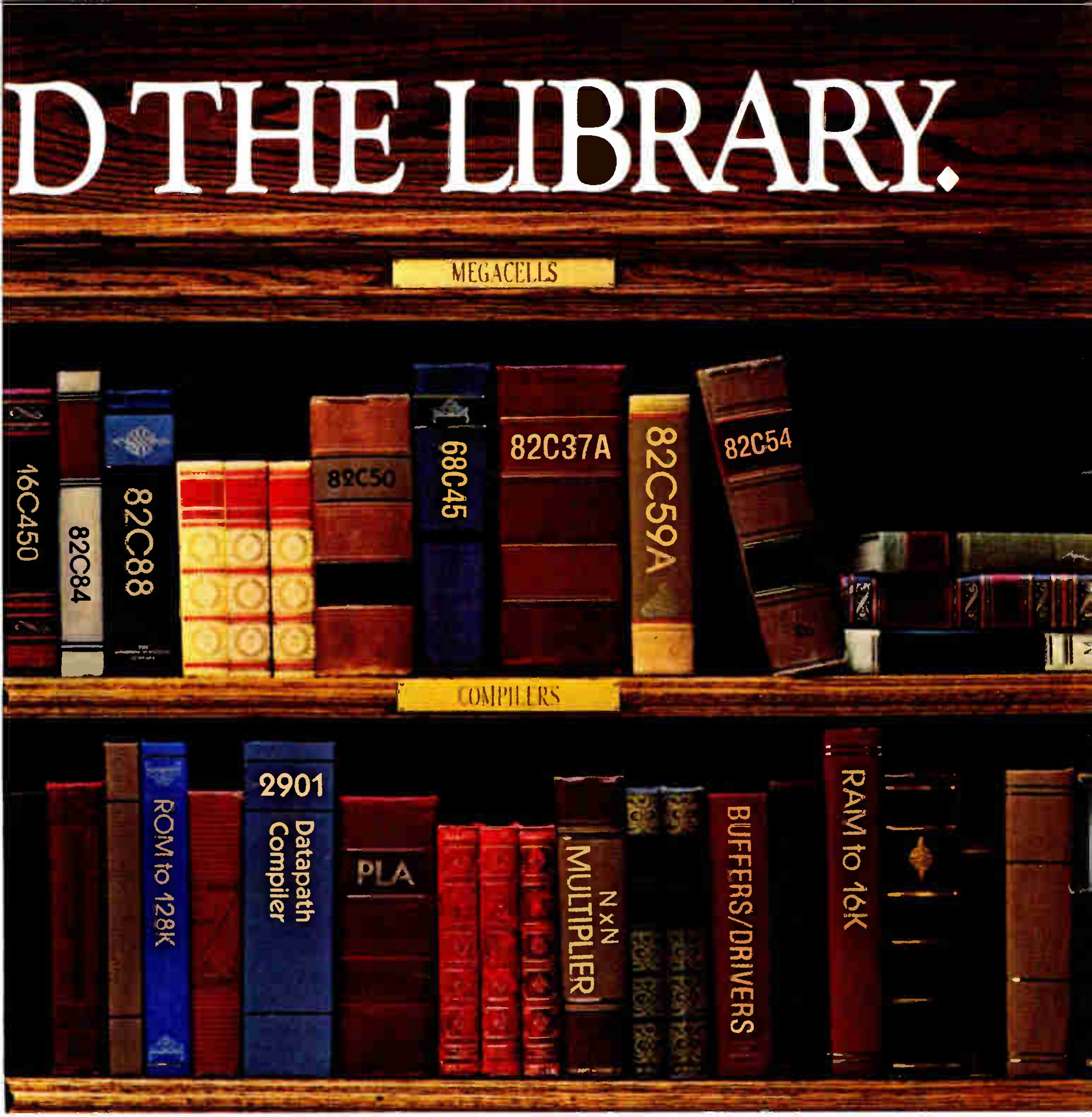

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D. Free distribution by mail, carrier, or other means samples, complimentary, and other free copies	8,604	7,565
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HOBBS QUITS 'GOOD LIFE' TO STRUGGLE IN STARTUP

BRIDGEWATER, N.J.

Roger Hobbs didn't wait to consider the question. "No," he said. "I never failed at anything." That kind of confidence prompted startup Quadtree Software Corp. to lure Hobbs from his plush quarters as a Burroughs Corp. vice president to the earthier role of chief executive at the struggling new firm.

Hobbs may miss some of the perquisites at Burroughs, but he's willing to sacrifice in the short-term for the hefty rewards Quadtree could reap in the future. "Roger has always had a desire to run businesses," he says, referring to himself in the third person. "Roger has twice built businesses. Roger is convinced he can do it again. But Roger wants to be paid for it."

Quadtree is banking its future on design-automation software for systems designers. The two-year-old Bridgewater company's software simulation models of off-the-shelf digital devices include such complex chips as Motorola's 68010 microprocessor. The market is new and for the most part uncharted, and it is one that Hobbs maintains is still "ill-defined." His job will be to define it.

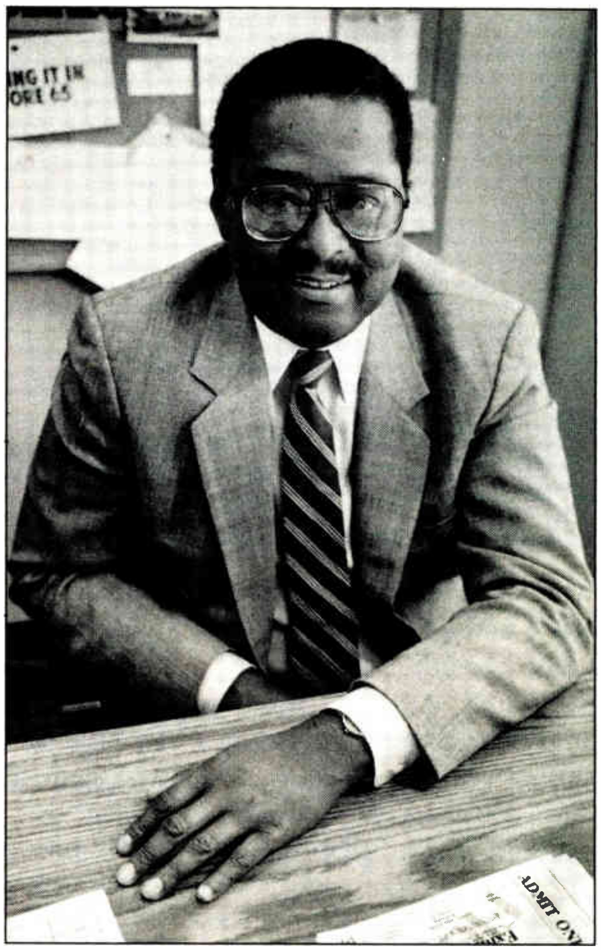
Hobbs, 43, brings 20 years of marketing know-how to a company he says is already "all over the technology." He knows, however, that technology alone will not guarantee success. "The challenge before us now is in the short term," he says, and that means building a marketing and sales organization, targeting the channels of distribution, and determining how to reach out to different kinds of customers.

It is just the spot Hobbs had been waiting for. Since graduating from Morgan State University in Baltimore in the early 1960s with a degree in mathematics, Hobbs has twice guided fledgling businesses to growth and success. With Quadtree, however, he faces a new challenge: working without the abundant resources of a large corporation. He doesn't seem at all worried. Hobbs is excited about going into a company that he can shape to his specifications.

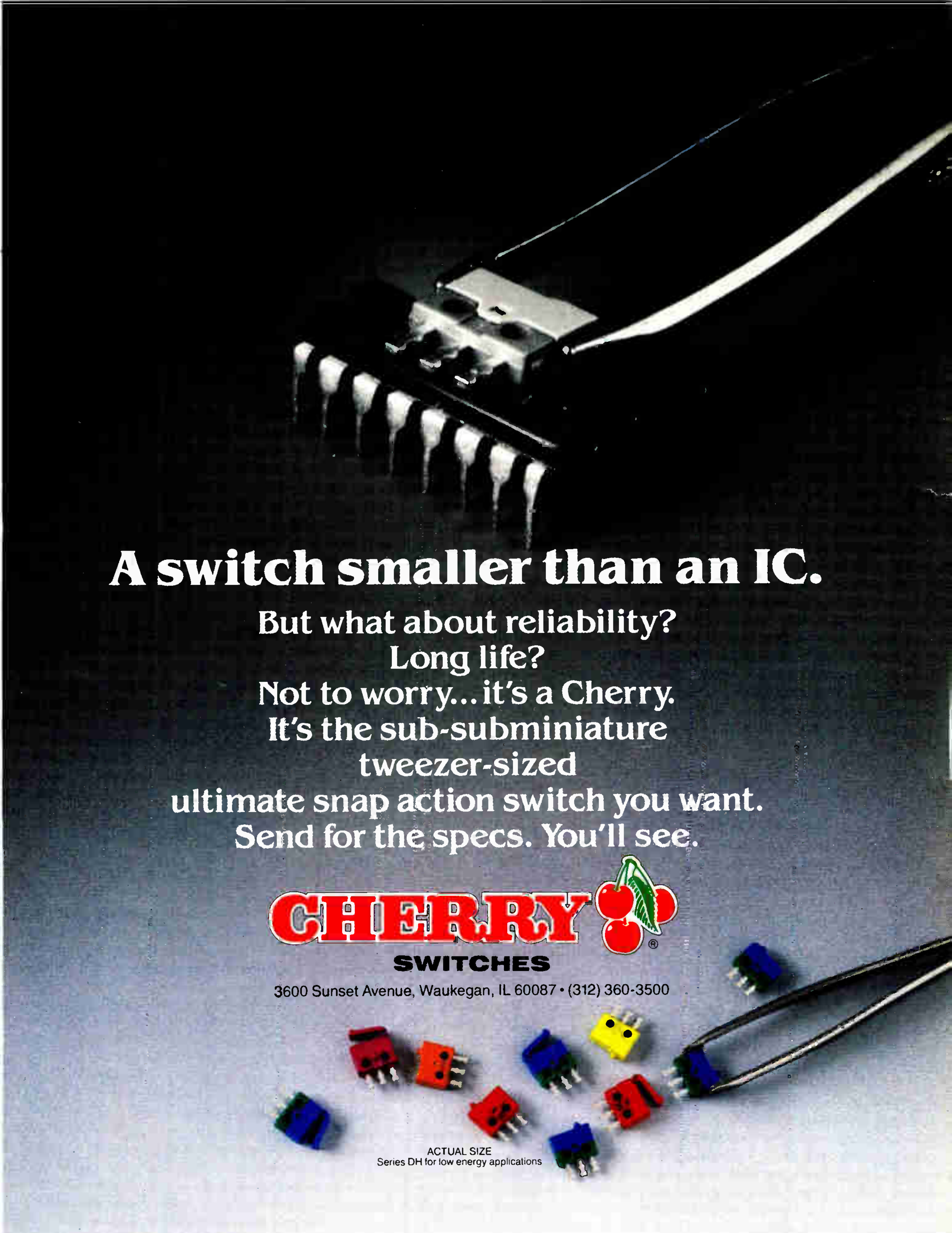
STARTERS. Hobbs began his career as a software analyst at AAI, a Baltimore defense contractor, but soon switched to sales at General Electric Information Services Co.—Geisco—in Rockville, Md., which offers computing and network services, mostly to companies too small to have such installations of their own. It was his true calling. By 1975—eight years after he started—Hobbs was named vice president for national marketing. Business more than doubled over the next five years.

Later, as vice president of strategic planning and acquisitions, Hobbs "learned to take a longer-term focus and to see things from a more global perspective." He also helped Geisco triple its sales in two years.

Hobbs moved to Burroughs in 1982 to



HOBBS: "Roger has always had a desire to run businesses. Roger has twice built businesses. Roger . . . can do it again."



Circle 15 on reader service card

The right vendor can put ASIC in a whole new light.

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put together a new software and services operation. He says, "They gave me an opportunity to have full responsibility for an organization, and that's what I wanted. By the time he left, he adds, "they had an operation that was going to produce."

He hopes now to achieve the same kind of results in New Jersey at Quadtree. "It's my objective to make us No. 1 in this business," he says. "I've got an insatiable appetite to drive for growth—and I'm convinced that that's what we need." *–Tobias Naegele*

KAHN AND CERF PURSUE 'A CIVILIAN ARPANET'

For more than two decades, the Defense Department's Advanced Research Projects Agency has been the prime source of funding for research in artificial intelligence, and the prime developer of the kind of computer networking techniques that are only now beginning to emerge in the commercial marketplace. Darpa kept AI alive when its commercial possibilities were only a dream; the Arpanet transmission-control protocols/internet protocols have been widely adopted in local networks while the International Standards Organization has slowly been working out its own protocols, which still haven't been fully implemented.

Two of the principals behind the Darpa research have now joined forces in a private research project that has as its goal nothing less than the creation of a national "information infrastructure" that would support computer communications in much the same way that railroads and highways support transportation, or in which the electrical power grid supports complex, nationwide energy use.

Robert H. Kahn, who crowned Darpa's AI program with the 1983 Strategic Computing Program for development of machine-intelligence technology, is the founder of the nonprofit Corporation for National Research Initiatives, in Washington, D. C. His longtime colleague Vinton G. Cerf, principal architect of TCP/IP and later the creator of MCI Mail, was his first employee.

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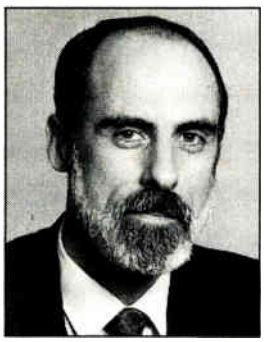

CERF. "He will drive you nuts asking for details."

Cerf and Kahn wrote the original TCP/IP paper in the May 1974 issue of the *Transactions* of the IEEE. Kahn has developed a reputation as a visionary who has seen the direction for computer science research, while Cerf is known as a genius at practicality. "He will drive you nuts asking for details," says Arpanet veteran Daniel C. Lynch.

Kahn, 47, left his job as head of the information processing techniques office last October, after a 13-year career with Darpa. Cerf, 43, detoured through MCI Corp. from 1982 to 1986, after six years as principal scientist for Kahn's office. With another Arpanet colleague, Keith Uncapher of the University of Southern California's Information Sciences Institute, they are creating a kind of civilian Arpanet.

The NRI will cultivate sources of income in the private sector for long-term research and development work on the information infrastructure, Kahn says. For starters, the organization has commitments for half a million dollars a year from Digital Equipment Corp., Xerox Corp., and several other major corporations.

The research will be done at universities or private companies, with NRI serving as the lead organization. Kahn has outlined three initial projects for which NRI will fund research: a national "knowledge bank" to codify know-how, much as an expert system does for an individual branch of knowledge; a digital library system, accessible electronically; and an electronic transaction framework.

However, Kahn cautions, the initial projects are still very experimental. No one knows what a knowledge bank looks like. "There are a lot of data banks that contain things you can retrieve," he says. "A knowledge bank will enable the knowledge that produced the data to be retrieved."

A further challenge, Cerf adds, will be in satisfying the sponsors. NRI eventually wants to administer an annual budget of $100 million in research projects. The big problem, he says, will be how to make the results widely available and still valuable to the companies that have put up the money. *–Clifford Barney*

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ELECTRONICS NEWSLETTER

A NEW TYPE OF PROGRAMMABLE LOGIC SEQUENCER IS COMING

In the first major variation of its programmable-array-logic architecture, Monolithic Memories Inc. has produced working silicon for a new kind of programmable logic sequencer. The Santa Clara, Calif., company plans to introduce Prose (programmable sequencer) in the first quarter of next year. Prose is designed to simplify the development of custom direct-memory-access controllers, disk-drive data formatters, and other high-speed state machines. The 25-MHz, 24-pin, fuse-programmable bipolar chip contains a 14-input PAL, a 128-by-21-bit programmable read-only memory that stores control bytes and next-state commands, and registers that put out the control bytes to the host system and feed back commands to the input section. Basically, the new architecture attacks the problems of using PROMs efficiently as state machines. Like conventional programmable logic sequencers, the Prose architecture couples a programmable-AND array to a programmable-OR array, but one is in the PAL and the other in the PROM. □

THE FIRST THIRD OF A 32-BIT GaAs RISC CHIP IS RUNNING AT TI

Texas Instruments Inc. is initially trying to fabricate in three steps what will end up as a single 32-bit gallium arsenide processor chip. Under development for the Pentagon, the first portion has already been built and is running as a separate 512-bit register file. The experimental 16-by-32-bit chip, containing 3,362 internal gates and measuring 120 by 180 mils, is believed to be the industry's largest working bipolar GaAs circuit, say TI project managers in Dallas. The register file, which has access times as low as 4 ns, was made to demonstrate 30% of a larger 32-bit reduced-instruction-set computer chip containing some 10,000 gates [*Electronics,* June 9, 1986, p. 21]. Although TI did not intend to offer the register file as a product, some customers have expressed interest in the device for military equipment. □

AT&T/YALE TEAM SEEKS EASIER WAY TO PROGRAM PARALLEL PROCESSOR

AT&T and Yale University researchers are joining forces to produce a high-speed parallel computer that is also relatively easy to program. Merging Linda, a set of software primitives developed at Yale that supports parallel programs written in C or any other conventional language, with S/Net, a prototype parallel architecture, researchers are now working to improve performance by producing a custom Linda chip—a very-large-scale integrated circuit that essentially incorporates Linda in hardware. The Linda primitives provide for a kind of shared memory called "tuple space," which is available simultaneously to multiple processors. But the AT&T-Yale implementation has no shared memory bank; rather, it is made up of multiple nodes in a communications network. □

MICROWAVE TRANSISTOR HITS RECORD 230 GHz FREQUENCY

The University of Illinois and General Electric Co. have combined to develop a microwave transistor with a maximum cutoff frequency of 230 GHz. They say the previous published record was 220 GHz, for a device fabricated by MIT Lincoln Laboratory in Lexington, Mass. Their modulation-doped field-effect transistor (MOD FET), built at the GE Electronics Laboratory in Syracuse, N. Y., also exhibits extremely high performance in two other parameters, says Alan W. Swanson, manager of the lab's advanced materials and devices section: low noise at 2.3 dB, and a measured maximum efficiency of 28%, when measured at 60 GHz. That compares with 2.5 dB and 14% efficiency in the best conventional AlGaAs/GaAs MOD FETs built by GE. The device relies on a 0.25-mm gate. □

ELECTRONICS NEWSLETTER

TWO NEW 1987 SEMICONDUCTOR FORECASTS: UP 5% TO 10%

Just when semiconductor watchers thought they had all the uncertainty they could handle, along come two respected Scottsdale, Ariz., industry consultants with 1987 forecasts that do little to make the crystal ball any clearer. In-Stat Inc. and Integrated Circuit Engineering Corp. are putting the finishing touches on the scenario each expects in the U. S. market next year—and their projections do not agree. In-Stat's president Jack Beedle thinks growth will not top 5%, largely because of a continued doldrums in computers. But ICE's vice president William J. McClean puts the figure closer to 10%, citing depleted inventories as a spur to growth. As if that weren't enough, the two really diverge on their early predictions for 1988. Beedle fears the bottom could drop out once again for U. S. semiconductor sales, with perhaps a 9% reduction. McClean believes a double-digit increase might be in the offing. ☐

MAKING ULTRATHIN EPITAXIAL LAYERS FOR COMPOUND SEMICONDUCTORS

Researchers at the Northwestern University Technological Institute in Evanston, Ill., have modified vapor-phase epitaxy to make thinner layers in multilayer compound semiconductor and optoelectronic devices. Existing systems rely on large vapor chambers for building structures on the order of 1 μm thick; they can't provide the precise control needed to grow the 10- to 100-Å-thick layers necessary for superlattice-based parts of the future. But the Northwestern researchers use a much smaller vapor chamber having a constricted growth area only about 2 cm in diameter. In addition, they force vapors through the growth chamber at high velocities and quickly vent them, further adding to the precise control of growth. So far, the team has built structures of about 100 separate layers, each 100 to 500 Å thick, with indium phosphide and indium arsenide phosphide. The technique could be ready for commercialization within two or three years. ☐

A GaAs RECEIVER CHIP WILL HANDLE GIGABIT-A-SECOND DATA RATES

A highly integrated transimpedence receiver, squeezing onto a single GaAs chip what has required an entire board, promises to bring gigabit-a-second optical networks within reach of a variety of applications. Microwave Semiconductor Corp., a Somerset, N. J. subsidiary of Siemens AG, has built the receiver chip, which is capable of handling 1-Gb/s data rates. The heart of such systems—high-speed lasers and p-i-n diodes that can bounce beams of light through optical fibers at gigahertz frequencies—are already widely available. The chip, part of a new family of GaAs chips introduced last week that support high-speed optical nets, is aimed at military aircraft applications. Product marketing manager James Herman says the parts could also make it in telephony markets, such as the integrated services digital network, and eventually in the gigabit-per-second home nets. ☐

SPERRY, LIKE IBM, TRANSFERS MAINFRAME POWER TO A MINI SERIES

Sperry Corp. is adapting the architecture of its OS 1100 mainframe computers to create a minicomputer family, and it unveiled its new line last Thursday, just two days after a similar IBM debut. However, Sperry will start shipping its new 2200 series in November; IBM's projected first deliveries for its new 9370 are a year away (see p. 33). The Blue Bell, Pa., company says the full mainframe is implemented on six 1.25-μm CMOS chips, each with 40,000 gates and 163,000 transistors. The first in the line, the 2200/200, comes in four models: the 201 single-processor entry-level system; the 202, with dual processors; the 203, with three; and the 204, with four. Prices range from $133,100 for the 201 to $381,700 for the 204. ☐

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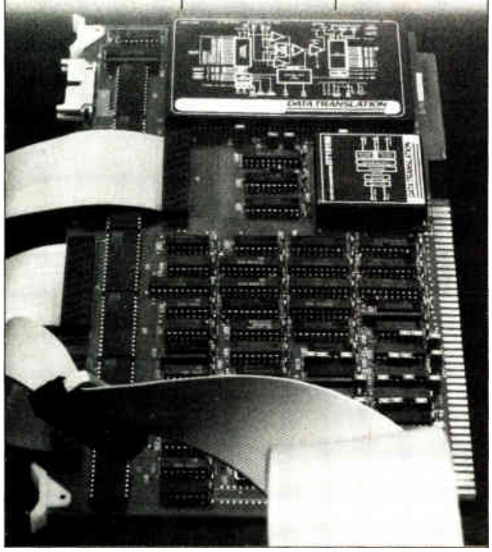

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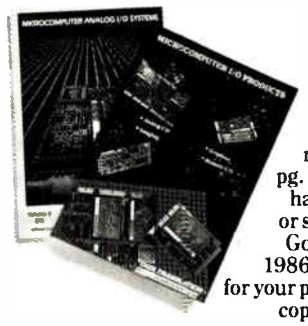

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PRODUCTS NEWSLETTER

PULSE GENERATOR RUNS FAST ENOUGH TO TEST GaAs DEVICES

Configuring equipment to test speedy GaAs devices has highlighted an urgent need for pulse generators with repetition rates in the multi-gigahertz range. That's why Colby Instruments Inc. is introducing its PG5000A, with pulse-repetition rates up to 5 GHz and rise times of 30 ps or less. The PG5000A delivers 2-V pulses on each of two independent outputs and costs $17,500. The Santa Clara, Calif., company will also offer it in two less-expensive models that package the generator as a separate clock-driver module for easier integration into existing systems. They cost $4,800; one has a single-ended output with trigger output, and the other a dual-channel output without trigger output. The pulse generators can also drive high-speed power laser diodes in communications equipment, the company says. □

TWO BEAMS SPEED UP FUJITSU'S WRITE-ONCE OPTICAL DISK DRIVE

Trying to pull ahead of the pack in the race to lead the 5¼-in. optical-disk market, Fujitsu America Inc., of San Jose, Calif., is adding a two-beam read/write laser to its write-once M2505A drive. The write beam inscribes information a fraction of an inch ahead of the read beam, which can immediately read it to detect errors. Moreover, errors can be corrected in the same revolution. Single-beam drives require two revolutions to complete a read-write cycle. The system also increases data integrity by using a photodetector to keep the read/write head vertically in focus and horizontally aligned over the area being accessed. Offering 300 megabytes of storage, the drive turns at 1,800 rpm and has a rotational latency of 16.6 ms and an average access time of 100 ms. Competitive drives currently store around 200 megabytes, spin at 1,200 rpm, and have a rotational latency of 25 ms and an average access time of 220 ms. The M2505A will be available in the first quarter of 1987 for $2,850 in OEM quantities. □

AMPHENOL SHRINKS OPTICAL PHASE MODULATOR

To get a jump on the guided-wave optoelectronic component market, Amphenol Products, a Lisle, Ill., operating unit of Allied-Signal Inc., is introducing a solid-state optical phase modulator built on a lithium niobate substrate. The Lini-Guide 747 Series comes in a 1-by-0.82-by-0.39-in. package with two fiber-optic pigtails attached. $LiNbO_3$ optical-waveguide devices offer potential for much faster optical modulation and switching speeds than are possible with conventional electrical devices [*Electronics,* Jan. 13, 1986, p. 20], and Amphenol says the Lini-Guide's small size will be particularly important for applications such as fiber-based gyroscopes. Lini-Guide components that operate at modulation bandwidths from dc up to several gigahertz are available now. The device is offered with nominal wavelengths of 830 nm or 1,300 nm; prices range from about $1,000 to $3,000. □

IBM DEVELOPS AN 80286-BASED SHOP-FLOOR COMPUTER

IBM Corp. will market a shop-floor industrial computer for manufacturing operations such as cell control and for gateway communications to Manufacturing Automation Protocol networks. The IBM 7552 Industrial Computer, based on Intel Corp's 10-MHz 80286 processor, uses 3½-in. floppy drives to make it compatible with the IBM Personal Computer AT and capable of running PC-DOS software. Two versions of the 7552 will be available in the first quarter of 1987. The model 040 with 512 K of memory, seven expansion slots, and no disk drives will cost $6,770; the $9,370 model 140 adds a hard disk and floppy-disk adapter card plus a 10-megabyte hard-disk drive, but has only five expansion slots. □

PRODUCTS NEWSLETTER

WORK-STATION TOOL LAYS OUT 10,000-GATE CHANNELLESS ARRAYS

Until now, designers of application-specific ICs have not had work-station place-and-route tools for channelless gate arrays of more than 4,000 gates. But California Devices Inc. is increasing the limit to 10,000 gates with its Wise II, which will save a typical $50,000 charge and two-week wait for layout by a foundry. The Milpitas, Calif., company's tool runs on Daisy System Inc.'s Gatemaster and MegaGatemaster work stations. Wise II is available immediately. Although priced at $25,000 when purchased separately, the software can be incorporated in the company's nonrecurring engineering costs for customers who use California Devices's gate arrays. The company developed the channelless, or sea-of-gates, architecture two years ago when it realized that efforts to squeeze more gates into an array were bumping against physical limits of its 1.2-μm design rules. □

SELECTIVE ENCRYPTION CODE LOWERS COST OF PROTECTING LAN DATA

Syntek Inc. is introducing a data-encryption system that can secure specified data sets on a local-area network while allowing general access to other information. The Secure 2000 system codes information by tagging each data set with an individual key. Each key-distribution center supports as many as 800 user terminals. The National Bureau of Standards Data Encryption Standard algorithm is used for all data encryption. The Mountain View, Calif., firm says it offers a significant price-performance advantage over point-to-point encryption systems that rely on separate circuits to protect specified information. Point-to-point systems cost, on average, $2,500 per port; the Secure 2000 system has been priced at $1,495 per two-port packet communication unit, the company says. □

RECOGNITION EQUIPMENT LINKS 8- AND 32-BIT DATA-ENTRY PROCESSORS

Look for Recognition Equipment Inc. to add a data-entry system running AT&T's Unix operating system on Motorola 32-bit 68020 microprocessors. What's more, users will be able to switch data files freely between the new Tartan XP and the older Zilog Z80A-based Tartan machine running a proprietary operating system. Just as the Irving, Texas, company puts a single-board computer within the 8-bit Tartan box for each user terminal, so the Tartan XP networks its single-board computers inside its box. The XP attaches by RS-422 or RS-232-C cables to the 8-bit computer boards in the existing Tartan system and will be available with 12, 22, or 32 terminal ports. It will offer up to 16 megabytes of main memory and as much as 2.5 gigabytes of disk storage. The 8-bit Tartan hardware remains in the loop to handle terminal communications. Tartan XP prices will start at $20,000. The system will be introduced at next week's Data Entry Management Association Conference and Exposition in Las Vegas. □

VMX TRIMS VOICE-MAIL HARDWARE AND COST

Semicustom CMOS gate arrays, surface-mounted chip packaging, and high-density hard disks have helped VMX Inc. trim the size of its voice store-and-forward equipment. The Richardson, Texas, company's new 5000 series is 59 in. high and 22 in. wide—about 20 in. shorter and about a fifth the width of the current VMX III voice-messaging system. The price also has been trimmed. A VMX III with 64 telephone ports and the ability to record 82 hours of messages sells for $525,000; the new 5000 series with 87 hours of storage costs $393,000. Double-density Eagle disk drives from Fujitsu Ltd. have boosted the maximum recording time to 516 hours, compared with 170 hours on VMX's existing system. □

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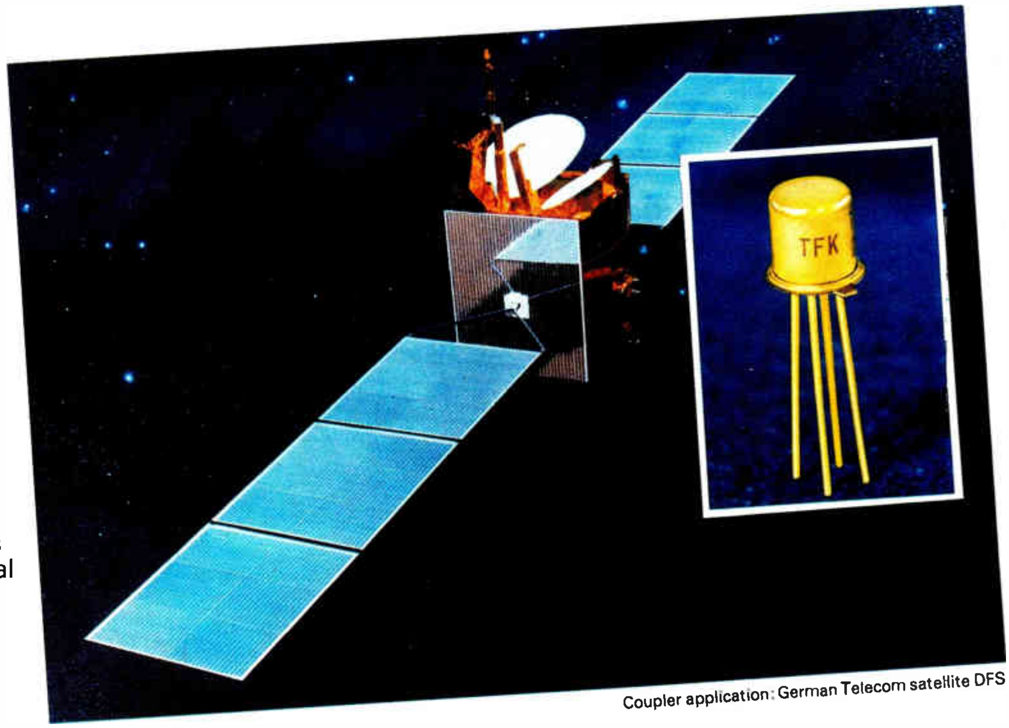

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Electronics

GATE ARRAYS MAKE AN END RUN AROUND MILITARY RED TAPE

DOD'S PART-QUALIFICATION PROCEDURES NO LONGER BLOCK THE WAY

LOS ANGELES

Surprisingly, gate arrays are beginning to make major inroads into military equipment markets. While the flexibility of gate arrays is just as big an advantage for military-equipment developers as it is for commercial users, that very flexibility makes using them in military equipment a procedural nightmare.

There are no military standards written for arrays, and those written for standard parts hinder more than they help. Because each finished gate array design is different in the final metalization layer, meeting military specifications for standard parts poses a major problem. Theoretically, the designer must qualify each design through the procedures and specifications that govern the procurement of standard off-the-shelf devices. Military equipment makers, however, are finding ways to get gate arrays through the specification thickets, such as the use of source-controlled drawings.

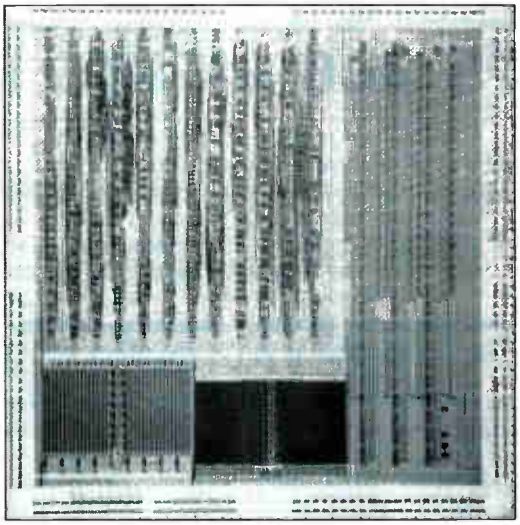
BOOMING BUSINESS. This has caused the gate-array business for military gear to boom. "Gate arrays are now picking up a real head of steam," says one vendor. "A significant upturn started 12 months ago and has turned even stronger in the past four months," says another.

By most accounts, the volume leader, LSI Logic Corp., Milpitas, Calif., will derive 20% to 25% of its overall revenue, or $40 million to $50 million, from military business. William J. O'Meara, vice president and chief marketing officer, says that nearly all new designs of military hardware are using gate arrays; there is what he calls "a mad rush" to these devices. Besides the density and power edge, the capability to deliver small quantities at a reasonable price makes the arrays ideal, in his opinion.

LSI Logic designed its first militarized CMOS array in 1982, and for several years 40% of all its new designs have been for the defense industry. Other companies selling CMOS arrays are General Electric, National Semiconductor, and VLSI Technology. Bipolar suppliers include Applied Micro Circuits, Fairchild Semiconductor, and Motorola.

Virtually every new military contract incorporates gate arrays, says Lanny Ross, vice president and general manager of Fairchild Semiconductor Corp.'s Gate Array Division in Milpitas. The suppliers have "done it without talking, but very quietly it has become apparent," he says.

Doing without specifications written for gate arrays, however, worries equipment makers. In cases where problems arise with equipment, documented adherence to a specification serves to limit the manufacturer's liability. No such official procedures now exist for gate arrays, although efforts are under way to set them up.



GETS SALUTE. LSI Logic's LCA10000 is a 1.5-μm CMOS gate array incorporated in many military designs.

Despite their concerns, equipment designers are succumbing to the attractions of gate arrays. Not only are the chips faster, denser, and less power-hungry than the boards of components they replace, but designs can be quickly moved from concept to silicon with the computer-aided-design techniques perfected for commercial customers. Especially useful are simulation procedures, which replace breadboard prototyping.

Many suppliers are using the same tactic to make up for the lack of gate-array specifications, Ross says: an acquisition procedure based on documents called source-controlled drawings, which are not often associated with semiconductors. This procedure can, in effect, replace meeting various military specifications, he says, when the buyer spells out performance, testing, and quality requirements in advance and the vendor closely adheres to them. When done correctly, the approach "will allow the military to buy anything," Ross contends.

In addition, gate-array vendors have improved their device fabrication lines so they comply with MIL-STD-883, which sets up quality requirements for component processing and testing. At Applied Micro Circuits Corp.'s plant in San Diego, Calif., for example, arrays destined for military use go through extra environmental screens, pre-burn-in tests, burn-in, and further screening before final testing and shipment. They thus meet all the processing and testing requirements existing for standard military circuits. The vendors are especially careful to observe those requirements, because for the gate arrays themselves "there aren't any rules, and that could be a problem," notes Michael Hollabaugh, AMCC maketing director.

Packaging also is a major hurdle, says Ron Hehr, applications engineering manager at United Technologies Microelectronics Center Inc., Colorado Springs. And most vendors have their own placement of power and ground, making second-sourcing difficult, he says.

The roundabout procedures being used may soon become unnecessary. A military specification for arrays is in the final preparation stages by the Rome Air Development Center, Rome Air Force Base, N. Y. It could be effective by the end of the year, according to Charles Windish, RADC project engineer. Under way only since late 1985, the effort to produce the document is intended to establish a military-wide generic standard for gate arrays. "Spec is a misnomer, since it is a quality-type procedure, really," says Windish of the document. *–Larry Waller*

MILITARY

MILITARY CHIP STANDARDS FACE SWEEPING OVERHAUL

ROME, N. Y.

The Pentagon is very quietly preparing to overhaul completely its qualification standards and procedures for procuring microcircuits and to replace them with a generally applicable set of generic qualifications and procedures.

Operating with funding from the Very High Speed Integrated Circuits program, the Rome Air Development Center, an Air Force installation in Rome, N. Y., signed a $5.24 million contract with General Electric, AT&T, and Honeywell last month to draft new standards and procedures. Design, fabrication, and test phases will all be affected.

The contractors will "revise our microcircuit qualification procedures and standards to make them more compatible" with application-specific integrated chips, says Maj. Rudolf Konegen, director of the VHSIC program at RADC. "We're embarking on a program to make the Joint Army-Navy procedures generic in the sense of process, test, and production."

The targets of these revisions are specifications prescribed by three standards. MIL-M-38510 is a general set of specifications; MIL-STD-976 covers procedures and standards for chip-fabrication facilities; and MIL-STD-883 requires that parts withstand certain environmental conditions, such as heat and humidity, and specifies test methods.

These standard procedures are time-consuming, expensive, and, some say, not necessarily the best way to guarantee that a given device will perform on the battlefield. "The old visual inspections at 100 × or 200 × are worthless. Some methods will not apply to VHSIC," says Bill Kritzler, the GE engineer who managed the contract proposal for the three companies and will now manage the program.

In addition, Kritzler says eliminating qualification testing, in which as many as 200 parts might be destroyed, could lead to shorter delivery cycles, lower-cost parts, and higher reliability. "The objective of the program is to tailor Mil Specs to the VHSIC world, to provide devices more cheaply and in a shorter time" by emphasizing procedural standards where parts are designed, rather than where they are fabricated, he says.

SOFTWARE MODELING. The program aims to use high-level software simulation and modeling in the qualification process so parts can be proven prior to manufacture. "With VHSIC, you don't get 140 parts to destroy during testing," Kritzler says. "Your lifetime order may only be about 140 parts."

A revised set of standards is due in September 1988, and within six months at least three VHSIC-class fabrication lines will be operating under the amended procedures. *–Tobias Naegele*

APPLICATION-SPECIFIC ICs

INTEL SWAPS 386 RIGHTS FOR IBM ASICs

NEW YORK

Intel Corp. has fortified itself with a multiyear technology-exchange agreement it has signed with IBM Corp., and through it hopes to become one of the top three producers of application-specific integrated circuits by 1990. Intel will rapidly adapt IBM's technology for use in its own products, rolling its first chips—a line of ten 1.5-μm dual-layer-metal CMOS gate arrays—off a new Santa Clara, Calif., ASIC line early next year.

IBM, for its part, will gain the right it has long sought to make its own version of Intel's powerful new 80386 32-bit microprocessor. Many industry observers believe IBM plans to use ASIC technology to add proprietary hardware to the 80386. Such a chip would become the heart of the next-generation Personal Computer, in a bid to fend off clone makers.

Details of the agreement were released last week. The deal was negotiated in the spring, but Intel and IBM tried to squash rumors of its existence until the announcement [*Electronics*, Oct. 2, 1986, p. 23].

To secure its slice of the semicustom ASIC pie—a market The Technology Research Group Inc. of Boston says will grow from $917 million this year to $8.26 billion by 1990—Intel plans to invest $75 million in its effort over the next three years. "By the end of the decade we hope to be in the $200 million [annual sales] range," says Jack C. Carsten, Intel senior vice president and general manager of its newly established ASIC Components organization.

With some 200 players in the ASIC arena, Intel has its work cut out. LSI Logic Corp., Milpitas, Calif., garnered

NCR-MOTOROLA ASIC PACT BEARS FRUIT

While Intel and IBM were unveiling their ASIC marriage last week, NCR Corp. and Motorola Inc. were celebrating the first major fruits of their 15-month-old union in application-specific integrated-circuit development.

The two companies announced the availability of a new 2-μm double-level-metal CMOS standard-cell library that is the first ASIC family to be developed jointly by the two companies. What's more, they unveiled a family of associated ASIC computer-aided-design tools that are said to be the first to allow full front-to-back-end ASIC design on a work station.

The new software tools will be available initially for Mentor Graphics work stations, with some pieces running on Daisy machines. The software is currently being used in NCR and Motorola design centers and will be fully available for customer use on their own work stations by early next year, says H. Gene Patterson, director of semicustom products for NCR's Microelectronics Division in Fort Collins, Colo. The package includes tools for the configuration and generation of high-level function blocks, layout, enhanced timing analysis and design verification, and test generation.

The tools will support the new merged 2-μm cell library, which initially includes 140 stand-alone cells. The library is built in an n-well process that is compatible with Motorola's 68HC05 microprocessor, the core of which is one of several complex cells that NCR and Motorola plan to add to the library by early next year.

Other cells due at that time include a cathode-ray-tube controller, a universal counter, a universal shift register, a multiplexer, and an arithmetic-logic unit. A dual-port random-access memory, a programmable logic array, and a Small Computer Systems Interface cell are to follow later next year.

The new library will supplant the 2-μm p-well-process CMOS cell library that was transferred from NCR to Motorola after the firms' link-up last year [*Electronics*, July 29, 1985, p. 20]. The new 2-μm library is ultimately capable of being shrunk to 0.5 μm, says Patterson. A 1.5-μm version should be ready for prototyping about mid-1987. *–Wesley R. Iversen*

$150 million in gate-array sales in 1985 to lead the pack with a 20% market share. "If we grow as fast as LSI Logic did, we'll meet our goals," says Carsten.

The pact should help. "It's a good deal for Intel, getting them out of the chutes running. Getting caught up on software, simulation software in particular, is what takes a lot of time to get launched in the ASIC marketplace, and Intel's got a good launching pad with IBM," says Millard Phelps, an ASIC market watcher at Hambrecht & Quist, San Francisco. "What IBM wants out of it would have to be the cell library comprised of a lot of [Intel's] megacells." IBM has already gained access to the cell version of Intel's 80C51 microcontroller and cell equivalents of microprocessor peripherals such as interrupt and direct-memory-access controllers.

DESIGN SOFTWARE. The 10 gate arrays IBM is handing over include eight with densities ranging from 2,500 to 19,500 gates, as well as two composite arrays that combine standard gates with 2,304 bits of on-chip static random-access memory. In addition to the gate arrays, Intel will receive rights to IBM's macrocell library, design software, and packaging technology.

The macrocell library, which provides the basis for designing with these arrays, consists of more than 100 logic functions. In terms of design software, Intel gained rights to "basically everything IBM has in relation to this gate-array technology," says Carsten. Most notable is IBM's hefty set of tools dubbed the Engineering Design System. Intel will use the tools for automated layout, test-vector generation, fault simulation, and mask generation.

Intel's customers will perform schematic capture, simulation, and timing verification using either IBM's newly announced Computer-Integrated Electronic Design Series environment or Intel's Integrated Design Environment.

Intel also gains IBM's packaging technology, which is called C4, for Controlled Collapse Chip Connection. Using solder-bump bonding techniques, this packaging makes possible ASIC packages with up to 183 pins.

Intel's field sales force will market the ASICs. Customers will receive training and assistance in the design of the semicustom chips at three facilities planned for Santa Clara, Boston, and Swindon, UK. The Santa Clara design center opens Oct. 15; the Boston and Swindon centers will open in December.

IBM, though characteristically mum, acknowledges it's happy to gain access to the 80386. "The agreement calls for us to have access to Intel's microprocessors and peripheral devices. That's what we get out of it," says spokesman Earl W. Inman. *–Alexander Wolfe*

IBM'S 370 ARCHITECTURE FINALLY GOES MIDRANGE

NEW YORK

Last week IBM Corp. took a big step toward solving one of its knottiest product problems. The Armonk, N. Y., company introduced its new 9370 Information System, bringing its successful System/370 mainframe architecture down into small-minicomputer territory. When the new series arrives, IBM says that it will have the broadest performance range for a single architecture—a ratio of 100 : 1 between the high-end 3090 model 400 mainframe and the entry-level 9370 model 20.

IBM midrange customers currently have to choose between the System/36 and System/38, neither of which is 370-compatible. The confusion of competing IBM architectures has left the company vulnerable to competition from Digital Equipment, Data General, and other minicomputer makers.

While industry analysts see the new products as a strong move by IBM to meet that competition, the new midrange models won't be arriving for some time. Shipments won't begin until the third quarter of 1987; the competition can make a lot of hay in 12 months of sunshine. And some of the software for advanced distributed processing also announced won't be ready until the fourth quarter of next year, IBM says.

LATE SHOW. At Digital Equipment Corp., Dave Korf, multivendor network marketing manager for the Maynard, Mass., company, emphasizes the late availability of the new IBM products. "Digital has a total solution right now," he maintains. "I don't think we'll see any pressure as a result of [IBM's] announcement."

A spokesman for Data General Corp., Westboro, Mass., agrees. "We're already into the second generation of departmental processors. Here they come a year from now introducing their first generation."

George Colony, IBM watcher and president of Forrester Research, Cambridge, Mass., agrees the new products are late. And he adds that they are expensive and confront end users with VM, a rigid and complex operating system. But the 9370 will be the right product for a lot of Fortune 1000 companies, he says. "IBM now has a compatible platform for easy-to-use office-automation software and departmental software."

The machines are built with dense, high-speed bipolar logic chips. For example, the processor's cache memory uses a 9,000-bit static random-access memory with a 25-ns access time for data and a 2,000-bit 16-ns SRAM for the main-memory addresses of data in the cache. Up to 80 of IBM's new 1-Mb dynamic RAMs—which are MOS chips—are mounted on each memory card.

At the low end, the model 20 is priced at $31,000 for a 4-megabyte system designed to support 64 work stations. A fully configured model 20, including processor, console, 400-megabyte disk drive, and tape drive, runs about $62,500. Compared with the current entry-level 370-compatible machine—the 4361—the model 20 offers better performance at half the price.

The largest of the four new machines, the 9370 model 90, takes up the space of two filing cabinets, costs $190,000 with 8 megabytes of memory, and supports 384 work stations. It is the first machine to bring to market an air-cooled version of IBM's thermal-conduction-module packaging. One module houses the processor logic, cache memory, and control store.

In conjunction with its hardware announcement, IBM announced a series of price reductions for software. The prices of more than 90 programs for the 370 architecture will be varied with processor size and performance. This translates into a big savings for customers with small machines: for 9370 customers, it could mean a price break of up to 75%. *–Rick Elliot*

LITTLEST 370. Next year, IBM's 370 mainframe architecture will extend downward to the 9370 model 20.

MICROSYSTEMS

INTEL PUMPS NEW LIFE INTO MULTIBUS I LINE

BOSTON

An old horse with new legs has entered the computer bus race, and it could give the younger, technically more advanced entries a run for their money. The old horse is the 16-bit Multibus I, which last week got its new legs in the form of a card featuring Intel Corp.'s 32-bit 80386 microprocessor.

SWEENEY: Multibus I gets a big boost with the 80386.

The Santa Clara, Calif., chip maker has added several major products to its Multibus I line, after going all-out in recent years to develop and market the 32-bit Multibus II. The II was aimed at meeting the competition from other companies vying to establish their bus schemes as standards in the 32-bit single-board computer market.

"With the rush toward 32-bit buses, you tend to forget that Multibus I still accounts for 41% of the single-board-computer market," notes Tim Sweeney, Intel's Multibus I marketing manager in Hillsboro, Ore. "With these new boards, which cost $3 million to develop, we're announcing that Multibus I is not dead and has a long life still ahead of it."

The new Multibus I entries include four new 16-MHz 80386-based boards, six new 80286-based boards, and a new disk controller board. "We are offering the CPU boards to address Multibus I customers who are currently compute-bound and I/O-bound," Sweeney says.

TIMELY BOOST. Industry observers are generally bullish on Intel's renewed Multibus I effort. "I think Intel needed some kind of boost right now, so it's a pretty good move on their part," says Harry Henry, president of The Market Information Center, Marlboro, Mass.

There's some speculation that Intel had come under increasing pressure because of delays in offering production quantities of its latest microprocessors and Multibus II products. To buy time with restless customers, say some observers, the company offered an immediate migration path to its latest microprocessor. Henry thinks that Intel may have needed these new products to "keep the attention of the current Multibus I customers" on the 386 chip and prevent crossovers to competing Motorola chips and VMEbus products.

Rob Hughes, executive director of the Multibus Manufacturers Group in Aloha, Ore., has mixed feelings. On one hand, the 80386 products could extend the life of Multibus I up to eight years. "But," he says, "I was also surprised to see no announcement on the Multibus II." Intel's Sweeney is quick to say that "the last thing we want is to have people walk away thinking that we're delaying Multibus II." Intel now says it will offer production quantities of the Multibus II 80386 products in the first quarter of 1987.

Intel is betting that a significant number of designers will opt in the short term to migrate to a hotter chip without scrapping existing bus architectures. Many customers within the $1.5 billion installed Multibus base simply want more performance without the hassle of redesigning backplanes. This is a trend Intel may not have foreseen.

The iSBC-386 line has an on-board 32-bit-wide bus that can connect with two memory modules, separate cards that fit onto the single-board computer in piggyback fashion. The 32-bit-wide bus makes possible 26-bit-wide addressing. To keep a low profile and fit inside a normal card slot in the Multibus I backplane, the DRAMs are surface-mounted on the piggy-back card.

The four piggy-back cards offer 1 to 8 megabytes of 32-bit-wide memory. Fully equipped with two 8-megabyte memory modules, the single-board computer provides 16 megabytes of dual-port program and data storage, allowing the central processing unit direct access to memory through a 64-K-byte no-wait-state cache.

ADDING ARITHMETIC. The 80287 arithmetic processor comes on some versions of the new computer boards. Intel plans to incorporate the new 80387 arithmetic processor when it becomes available. "The new line of boards will significantly extend the performance range of Multibus I without requiring the OEM to change his bus or backplane," Sweeney says. The 80386-based boards will be available in November and will range in price from $4,800 to $12,990.

Sweeney says Intel expects to ship more Multibus I 80386 cards in the short term, but he predicts that over the next five years the Multibus II 80386 products will pull ahead. The Multibus I line provides performance approaching that of Motorala 68000 products on VMEbuses, he notes. When Intel offers 20-MHz 80386 processors in the near future, performance should increase by 25%. *–Craig Rose and Jonah McLeod*

HYBRID CIRCUITS

MOTOROLA MAKES A RUN AT THE HYBRID MARKET

SCHAUMBURG, ILL.

There's a formidable new contender in merchant hybrid microelectronics. Following a growing industry trend, Motorola Inc.'s Communications Sector is unveiling plans this week to take its previously all-captive hybrid business to the outside. The company plans to concentrate initially on circuits for communications, consumer, and instrumentation equipment, says Dennis D. Reifel, director of new business for the Communications Sector's Manufacturing Group in Schaumburg.

By offering hybrid circuits to original-equipment manufacturers for the first time, the Motorola operation is out to establish itself quickly as a major player in the worldwide hybrid market, which the company predicts will total some $8 billion this year. Reifel has high hopes for growth, even in the short term, for Motorola. He expects to do $25 million in outside hybrid business next year. "And that," Reifel points out, "would make us bigger than two-thirds of the people already in the business."

Other Motorola operations already offer hybrids on the open market. But they're small change compared with the massive push planned by the Communications Sector. The new merchant business will be a separate operation, with headquarters in Plantation, Fla., that brings to the market 18 years of experience in building hybrids for Motorola's own line of portable radios and pagers.

EXPERTISE. The company has highly automated, high-volume hybrid design and manufacturing systems in place in Florida, Singapore, and Malaysia. And it's well-positioned to offer one of the broadest OEM capabilities in the business, Reifel says. Its expertise includes both thick-film and single- and multiple-layer thin-film technologies, and there is a choice of either chip-and-wire packaging or assemblies based on surface-mounted chip carriers. These can be employed on a variety of substrate types,

SIEMENS

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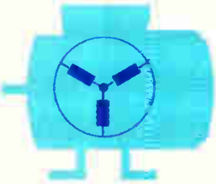

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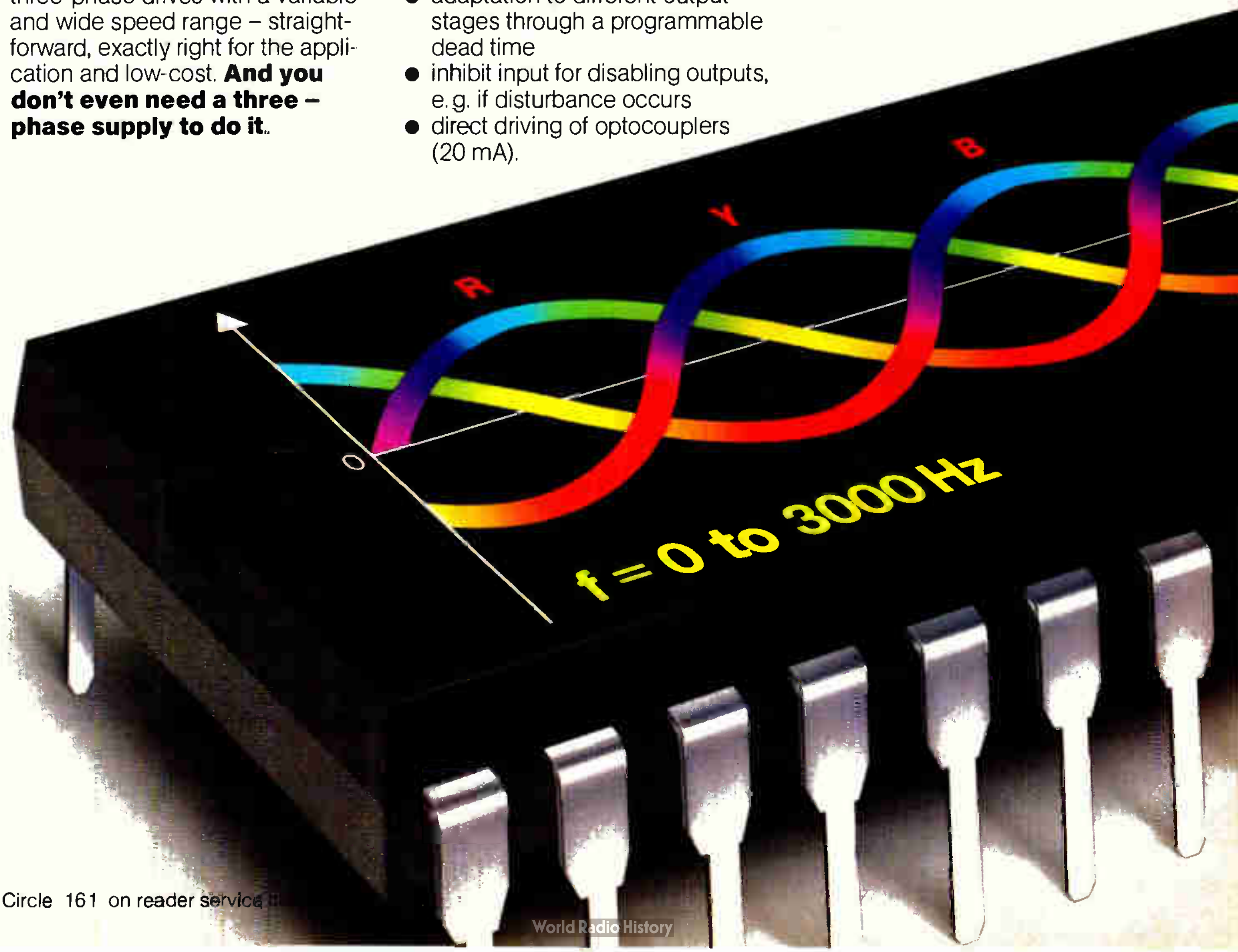
If you want to find out more about SLE 4520, write Siemens AG, Infoservice 12/Z016, Postfach 23 48, D-8510 Fürth, West Germany quoting "Pulse-width modulator".

12/Z016e



Circle 161 on reader service

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Circle 37 on reader service card

ranging from conventional ceramics and circuit-board materials to flexible laminates.

Motorola will put its emphasis on competitive pricing and high quality. "We'll be offering a three-year warranty, and I think that's an industry first. The norm in the industry is one year," says Gerald W. Blanton, director of operations for the Manufacturing Division in Plantation.

Outsiders agree that the new Motorola operation is likely to wield a big stick in a merchant business populated mostly by small job houses. "Motorola's entry could be very significant. There are about 350 companies in the [merchant] hybrid industry today, and fewer than two or three dozen of them are doing over $10 million a year," observes F. Peter Huntsinger, director of marketing and sales, hybrid components operations, for Tektronix Inc. of Beaverton, Ore.

REIFEL: Expecting $25 million in outside business next year.

About two years ago, Tektronix began offering hybrid circuits to the OEM market out of its now 17-year-old hybrid operation, which previously supplied only internal Tektronix needs. Huntsinger won't cite specific numbers, but he says Tektronix's OEM hybrid business is already running at well over $25 million in annual sales. Within the last 18 months, Huntsinger notes, other major captive hybrid operations have also started selling circuits to the outside, including those operated by AT&T Co. and Boeing Electronics Co.

The attraction is not hard to understand. According to a study published last year by the New York research firm of Frost & Sullivan Inc., the U.S. hybrid market alone will total $5.3 billion this year and will rise to $9.1 billion by 1989. Ross Stander, author of the report, expects a continuing trend by large manufacturers of systems to convert their hybrid operations from cost centers to profit centers by offering products on the open market.

Given the size and diversity of the hybrid business, Stander believes many independent hybrid suppliers will be able to maintain operations by serving specialized niches. But the entrance of more large-scale, previously captive vendors such as Motorola is also sure to put pressure on companies that can't afford to invest in automated design, manufacturing, and test equipment—driving some companies out of the business, Stander points out.

For its part, Motorola has completed four months of test marketing and is prepared to make capital investments at whatever levels are required to support the new business, Reifel says. The company already has its eye on several high-volume accounts, he says, mentioning European firms such as Siemens and North American Philips among prospective customers. In addition to opening sales offices in Plantation, Motorola's new OEM hybrid unit will sell circuits through a network of about 10 domestic and 26 foreign manufacturers' representative firms. Motorola expects to have that network in place by mid-1987.

–Wesley R. Iversen

SEMICUSTOM ICs

SEA-OF-GATES ARRAY PUTS 75% OF ITS GATES TO USE

SAN JOSE, CALIF.

In a move that is likely to further blur the boundaries between gate arrays and standard cells, VLSI Technology Inc. of San Jose has developed what it calls its continuous gate-array technology. The techniques used, which include space-saving epitaxially grown device isolation and transistor regions that can be used as part of an interconnect channel, can bring gate-utilization efficiencies close to that achieved in standard-cell designs—up to 75% to 90% at very large-scale integration densities, the company claims (see p. 53).

The standard approach for gate arrays, where interconnection can cover as much as 65% of the chip area, is to set aside areas for interconnect channels, even though many designs may not need all of this area. And at high densities—in excess of 25,000 gates—gate utilization drops to 25% or 30%.

To solve this problem, several companies have developed array structures in which the area set aside for interconnection incorporates structures that can be used as gates if interconnect lines do not run over them—a technique variously called sea-of-gates, channelless arrays, or abutted gate arrays.

This method doubles gate utilization to 50% to 60% at the 25,000-to-50,000-gate range, but at VLSI densities the efficiency begins to drop again. In some arrays in the 100,000-to-125,000-gate range, only 50,000 or so can be used.

In VLSI Technology's continuous-gate-array methodology, designers have pushed the sea-of-gates concept further to achieve 75% to 90% gate utilization. In the first family of devices to use this methodology, the VTG100 series, utilization efficiency remains constant with density increases.

STEADY RATE. For example, in a 12,000-gate array, the total number of usable gates is 9,000, and in a 66,000-gate array, it is 50,000. And in future higher-density versions, the same rate is expected to be maintained, if not improved, says product engineer Russ Steinweg. For example, in a 90,000-gate array in development, 70,000 to 80,000 will be usable.

Among the technology breakthroughs that make this possible in the VGT100 series is the array layout, says product manager Dan Yoder. It consists of long rows of alternating n- and p-channel transistors, called continuous pairs. Any of these transistors can be used either as an element in a gate or as part of an interconnect channel. Current sea-of-gates arrays have two types of areas, one exclusively for gates and the other for channels, but with the potential for implementing active gates where interconnection is not needed. In VLSI Technology's new arrays, this duality does not exist: there are no sections of the chip where interconnections cannot go.

One of the chief benefits of this structure, Yoder says, is that it allows the use of an automated global placement-and-routing algorithm with less restrictions imposed upon it. The algorithm, as a result, is comparable in speed and gate efficiency to those used in the fabrication of standard cells.

Furthermore, the company uses epitaxially grown gate isolation, rather than the usual diffused field-oxide isolation, to separate active regions. Diffusion cannot be controlled to the close tolerances possible with epitaxial growth; using grown isolation thus makes it possible to use smaller isolation structures. By freeing about 20% of the core area normally devoted to oxide isolation, the company can put more transistors on a chip of a given size.

Because the continuous-gate technology increases layout density and cuts interconnect length, performance also improves, Steinweg says. Fabricated using a 1.5-μm double-layer-metal fully implanted CMOS process, the VTG100 series runs at clock speeds up to 100 MHz. An internal two-input NAND gate with a fanout of two has propagation delays of no more than 700 ps and dissipates only 20 μW per gate per megahertz at 5 V.

–Bernard Cole

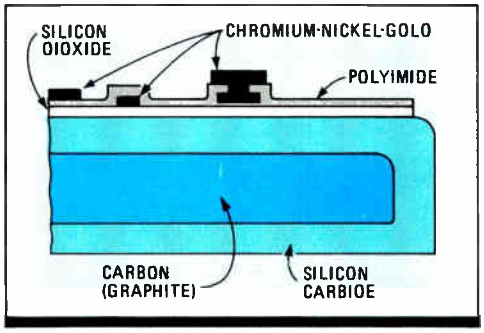
NEW TI SUBSTRATE AIMED AT MOUNTING FLIP CHIPS

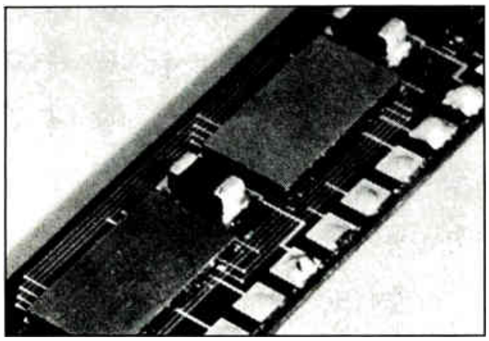
DALLAS

A new kind of circuit-board substrate that promises high circuit densities at relatively low cost is being studied seriously by Texas Instruments Inc.'s Semiconductor Group. TI's work on the substrate, which is made with silicon carbide and graphite, and on an associated chip-packaging technique pioneered by IBM Corp., marks an effort by the chip maker to investigate new packaging technology, rather than rely on variations of conventional packages such as chip carriers, small-outline packages, and pin-grid arrays.

The approach, in an early developmental stage at TI's process automation center in Dallas, is based on "flip chips," a technique by IBM. The flip chips have copper-and-solder bumps formed over their input/output pads during fabrication. Then the chips, mounted with the active side down, are reflow-soldered to the substrate.

Although TI has made no marketing plans yet, Walter Schroen, the department manager of packaging for semiconductor corporate research, foresees the substrate—now made as large as standard single in-line packages—used for multichip memory modules, as well as microprocessor and logic applications requiring three to nine chips. The multichip substrate can be built into another package or used as a subassembly.





THERMAL MATCH. TI's new substrate has a graphite core (at top). Chips are bump-bonded to it face down (right).

If flip chips are to be placed on a substrate, the substrate must have a thermal coefficient of expansion close to or equal to that of silicon. Without such a thermally compensated substrate, the shearing stress produced by the different expansions of the chips and the substrate during thermal-shock conditions would produce microcracks in the chip.

AT THE CORE. TI's custom substrate (see diagram) has a core of graphite and silicon carbide that matches the expansion coefficient of silicon. This developmental composite material has excellent thermal conductivity and low alpha-particle radiation, which is vital to prevent excessive soft errors in MOS memories. The substrate is hard and tough and costs about the same as printed-circuit laminates.

The substrate is batch-processed in a way that's analogous to processing a silicon wafer. Silicon carbide is deposited around an inner core of graphite. A layer of silicon dioxide is deposited as an insulator over the slightly conductive substrate. Then, fine-line thin-film conductors made of layers of chrome, nickel, and gold are laid down.

A two-layer interconnect pattern can be built up on the substrate with an integrated-circuit-grade polyimide used as the dielectric. This layering, along with the fine-line conductors and the use of flip chips, makes extremely dense packaging possible. *–Jerry Lyman*

HITACHI DEVELOPS ITS OWN 32-BIT CHIP

TOKYO

Hitachi Ltd. has been second-sourcing early members of Motorola Inc.'s 68000 microprocessor family for some time. But it has been unable to license recent advanced 32-bit microprocessor designs from Motorola. So, keeping its eye on the special performance needs of Japanese work stations, Hitachi is developing what it calls a second-generation 32-bit design that is compatible with other manufacturers' products at the Unix source-code and C-language levels rather than at the object-code level. The first versions of the chip are due at the end of 1987.

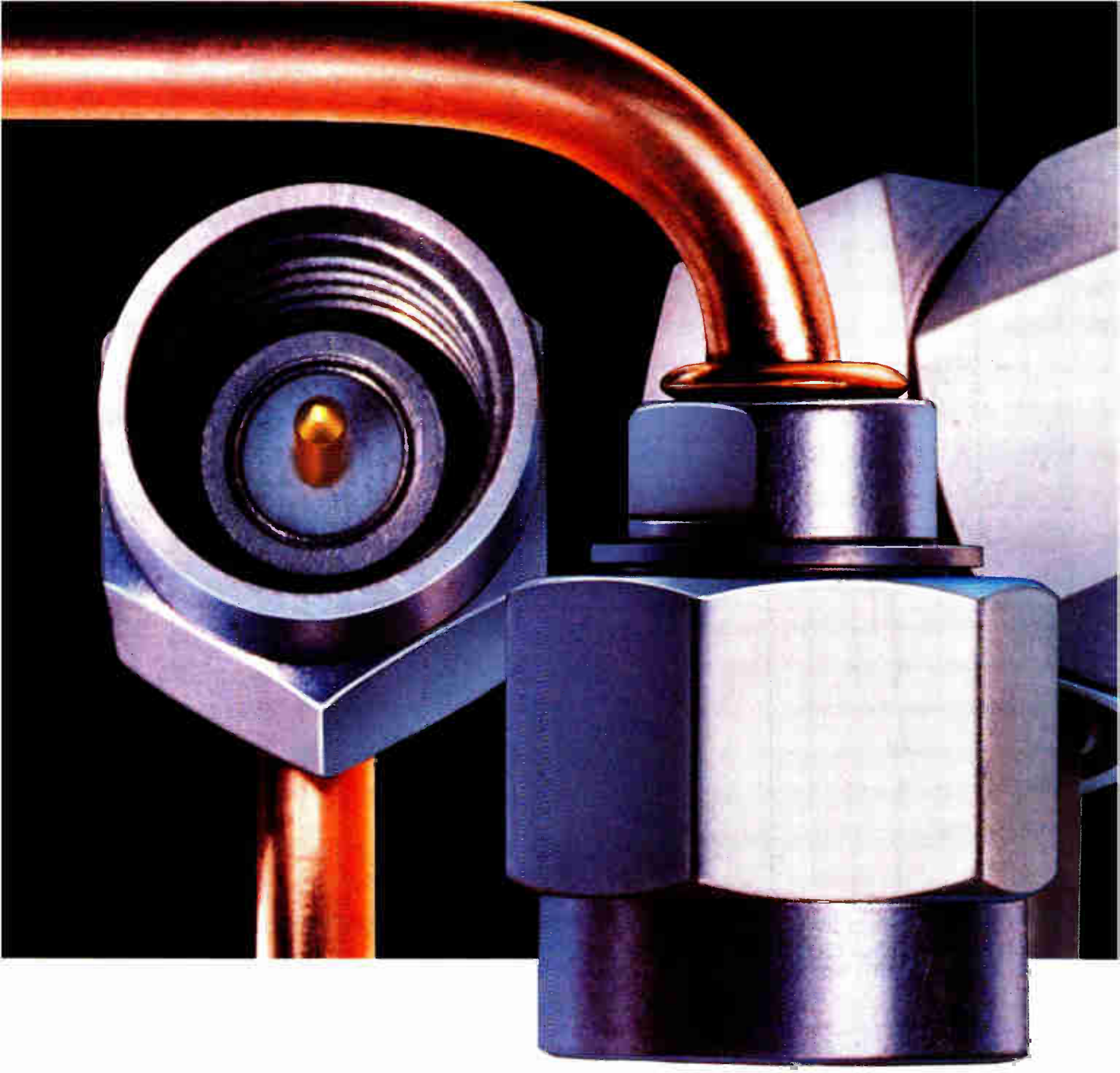
Although Hitachi says the new processor, called the H32, will be very fast, it is most notable for the family of chips that will surround it. Among those chips will be a processor that executes the intermediate code of artificial-intelligence languages, a floating-point coprocessor that can be tightly coupled to the H32, and 16-bit and 8-bit processors.

The H32 and its associated chips are targeted for high-end work stations, which Hitachi believes require enhanced performance and more functions than Motorola's chip set provides. The better performance possible with a proprietary design makes this route desirable for the Japanese market, according to Hajime Yasuda, manager of the Strategic Product Planning Department at Hitachi's Semiconductor and IC Division. Japanese customers require enhanced functions—many of them related to the complexities of the kanji language, such as those for graphic display—that existing 32-bit chip sets cannot provide, Yasuda says. The Hitachi design is primarily for Japanese market, but he is sure that there will be a worldwide market as well.

The company's experience in C compilers and the Unix operating system influenced the architecture of the H32 family, Yasuda says. Other parts planned for the set include a tightly coupled direct-memory-access controller and two chips that will be loosely coupled to the processor via the system bus and thus should work equally well with other 32-bit processors. These parts are a graphics data processor and a smart dual-port random-access memory. The AI-language chip, called the AI 32, is also to be loosely coupled to the H32.

FAST EXECUTION. The H32, implemented in 1.3-μm design rules, is scheduled for sampling at the end of 1987. The microprocessor will operate at a 20-MHz clock frequency, which will increase to 24 MHz when a 1.0-μm device is ready. The 20-MHz version is expected to execute up to 4 million Whetstone instructions/s in combination with a floating-point coprocessor.

Hitachi has also announced plans to build 8- and 16-bit processors that feature the same definition of C and thus are source-code-compatible with the H32. Designed for performance, they will be available initially with peripher-



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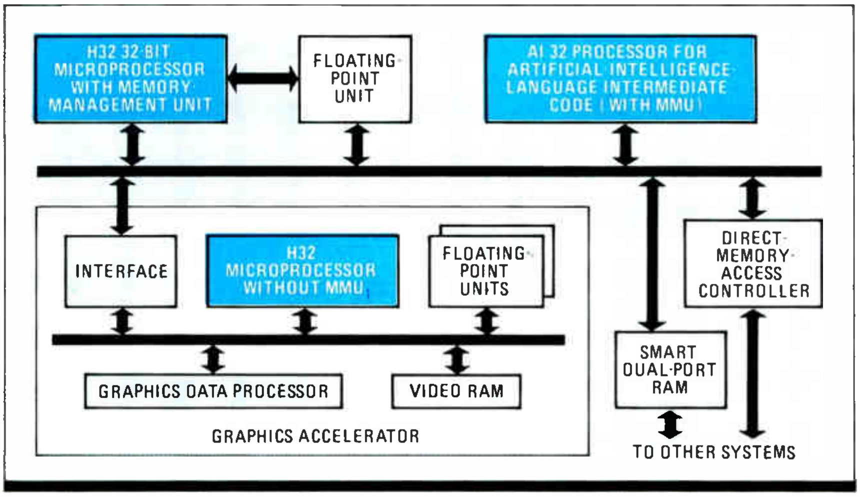


FAMILY PLANS. Hitachi has a 32-bit microprocessor and several companion chips on the way.

als on-chip for standard applications, but the company intends eventually to use them as cores in application-specific integrated circuits. Yasuda is especially proud of the H16, in which 16 sets of registers and bank switching of 16 memory areas will make context switching or procedure calls extremely fast.

Itron, a real-time operating system developed by professor Ken Sakamura of Tokyo University, will be the major operating system for the H16; Itron will also be used on the H8 in some applications. Btron, a version optimized for business applications, may be used on the H32, too. Itron will also be used on the H32, in addition to Unix.

The H32 features a 32-bit address bus for full linear addressing of up to 4 gigabytes. The 16 individual 32-bit registers on the chip can be used either for addresses or data, rather than half being dedicated for each function as in the Motorola 68020. A demand-paged memory-management unit can be disabled where it is not needed, as in graphics applications. There are two completely independent caches: a 1-K-byte instruction cache and a 32-word data stack. A 135-pin grid-array package will provide for separate data and address lines.

The floating-point unit, due at the same time as the H32, implements a 64-by-64-bit multiplication in hardware rather than microcode. It can be tightly coupled to the H32, but it is designed to yield high performance with other processors, says Yasuda.

Floating-point calculations and graphics are expected to be two of the H32 family's strong suits. For highest performance, the graphics-display process is accelerated by an H32 controller and up to eight floating-point units (see figure). Because the graphics subsystem is loosely coupled to the system bus, it could be used as efficiently with other microprocessors.

DEDICATED. The AI 32 is a dedicated microcoded processor that can directly execute the intermediate code of an AI language—Smalltalk-80, Prolog, or Lisp—so it becomes an inference engine for that language. Its microinstruction store is implemented as 4-K 128-bit words of erasable programmable read-only memory, allowing users to write their own implementations of AI languages (or configure the chip as a communications controller). Parallel language processing is enhanced by two register files of 256 40-bit words each.

Benchmark tests have shown this architecture to be 10 to 20 times faster than conventional architectures—such as that of the 68010—for execution of AI languages, and three to five times faster than reduced-instruction-set computer architectures, Hitachi says.

System designers can run efficient programs directly in an AI high-level language, rather than developing them in Lisp or Prolog and converting them to C or some other language to run on a standard processor. The AI chip is tentatively scheduled to be available by the end of 1987 also, the company says.

–Charles L. Cohen

DATA PROCESSING

RISC DESIGN DID NOT DELAY SPECTRUM

PALO ALTO, CALIF.

Hewlett-Packard Co. caused a great stir recently when it pushed back the first shipment date for its Spectrum business computer, but the trouble apparently does not relate to the machine's novel reduced-instruction-set-computer architecture. The computer maker's overly ambitious plans for the new operating system seem to have caused the problem.

"It's a very, very great disappointment to all of us," says Hewlett-Packard Co.'s Joel Birnbaum. "We apologize to everyone." Birnbaum is more than sorry; he is embarrassed. As vice president of research at HP and the leader of the Spectrum project, which will completely change the HP computer line with its RISC architecture, he has emphasized the thorough modeling, measuring, and testing that Spectrum has undergone. Spectrum, he declares, is not a risk but an engineered solution.

Nevertheless, HP bit the bullet and announced a six-month delay in shipping the first Spectrum business computer, the 3000 Series 930. Interfaces between the operating system and several other new software components led to a degradation of performance in the 930.

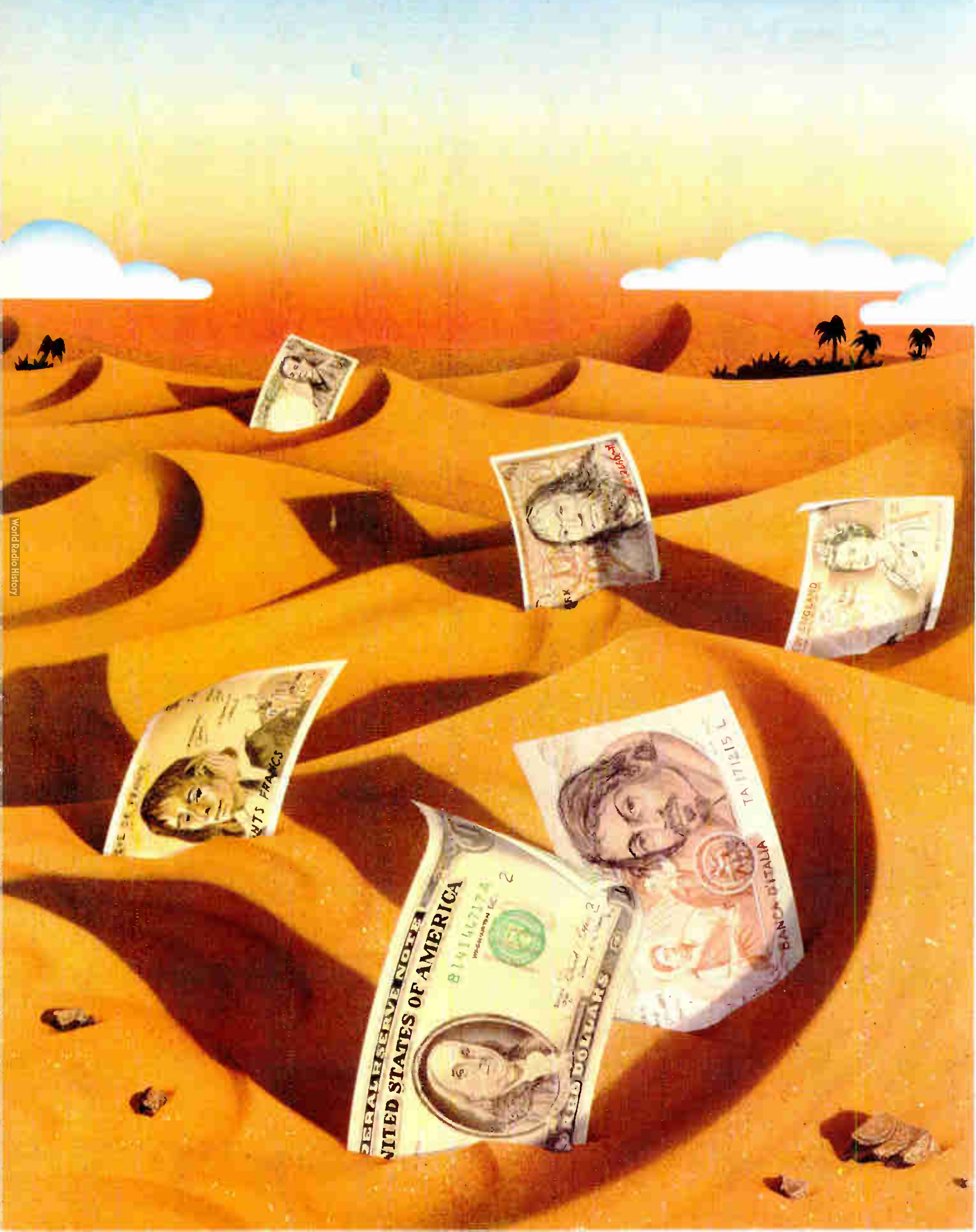
Hoping to mend some of the damage, HP noted that its first technical Spectrum computer, the 9000 Model 840 for engineering and computer-aided manufacturing, was still slated to ship on schedule, in December. The 9000's Unix operating system had no problems with Spectrum's memory-mapped input/output or its new database structures, but HP's proprietary operating system, called MPEXL, ran into trouble trying to swap data around.

BIRNBAUM: Spectrum hangup is only a software glitch.

To reassure customers who want to upgrade their 16-bit HP 3000s with the 32-bit, 4.5-mips machine, Birnbaum and a group of Spectrum executives flew to a users' group meeting in Detroit late last month. They reportedly met with a mild reception from customers, who accepted HP's word that the problem was not critical, but an annoying example of Murphy's Law at work.

Some industry watchers agree. Van Weathers, who tracks computers at Dataquest Inc., a San Jose, Calif., research firm, doubts the delay will hurt HP much. "For a vast majority of their customers, a six-month delay is not unreasonable," Weathers says. "It's not as if their entire installed base were running out of gas today." For those who do

The Hidden Costs...



need more capacity, HP has introduced a non-Spectrum upgrade, the Series 70, he points out.

But other observers, particularly on Wall Street, were more pessimistic. They thought the delay was a break for rival Digital Equipment Corp., and HP stock quickly lost 10% of its value on the New York Stock Exchange, in a generally declining market.

The problem surfaced several months ago, Birnbaum said, as HP started integrating all of its new software components and moving them to alpha sites inside the company. Users found that some customer application code made the instruction-path length—the series of decisions the operating system goes through to perform a filing operation, for example—unacceptably long.

COMPACT CODE. The problem was not one of a growth in the number of central-processing-unit cycles it takes to execute high-level-language instructions, Birnbaum added. This has been a key point in the arguments of RISC opponents, who say that its one-instruction-per-clock-cycle operation leads to unacceptably large programs. In fact, Spectrum's Cobol compiler produces code that is actually 20% shorter than code used in HP's older architecture, Birnbaum says.

However, adding the new software components reinflated the instruction-path length for operating-system operations in some circumstances. "The filing system, the data base, and the network also contribute to the path length," Birnbaum says. For example, HP's operating system keeps a map of the disk file, so it can bring data directly into main memory. The process simplifies I/O handling in general, but incurs operating-system overhead that is usually paid for by the data-base manager.

TUNING. Ultimately, HP expects the mapping of files into virtual address space to save on overhead, says Michael Mahon, manager of the computer languages laboratory. But first, operating-system primitives must be tuned so that frequently used primitives are near the top of a decision tree. This process is now keeping many of Spectrum's several hundred software engineers busy.

Birnbaum decided that the system must be delayed, although he downplays the problems: "We think that this is a performance glitch, not a technical problem. There will be no changes to the instruction set or the bus design, for instance. We are streamlining the critical path in the operating system and the data base, where we added so much function that it got out of hand. We think the six-month delay we have announced is the longest the job can take. We don't want to embarrass ourselves again." *–Clifford Barney*

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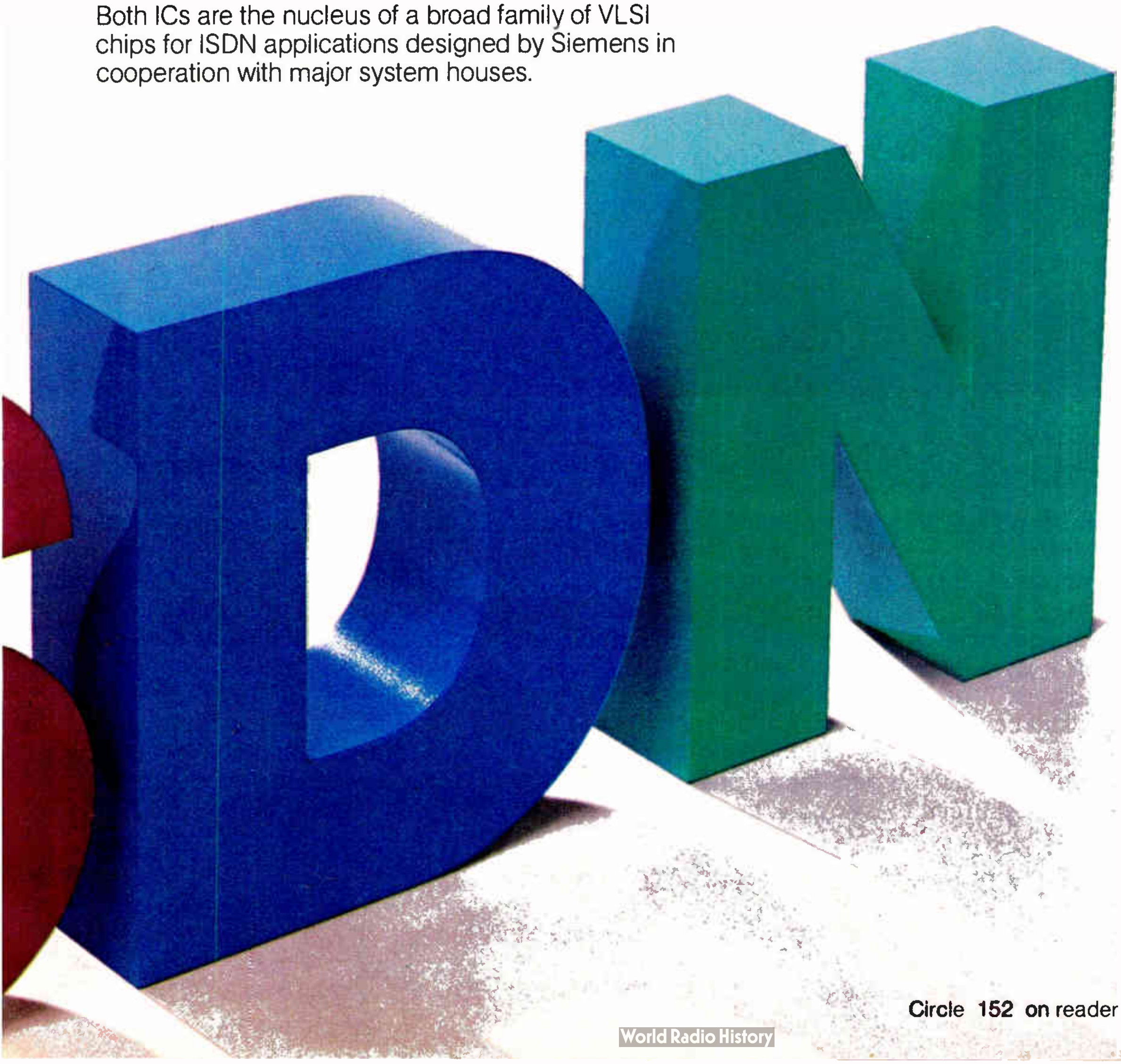

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NEW 32-BIT CMOS MICROPROCESSORS.

The two new members of NEC's CMOS microprocessor V-Series bring unprecedented density and performance in the 32-bit realm. The V60 and V70 supermicros are the first to integrate a Memory Management Unit and basic floating-point processing functions on a single chip.

The V60 has a 16-bit external data bus for an easy, affordable path into 32-bit products while the V70 is a full 32-bit engine designed to power leading-edge systems.

The super-fast V60 and V70 offer a clock speed of 16MHz, and execute 3.5 MIPS and 6 MIPS respectively. A six-stage pipelined CPU enables concurrent execution of up to 4 instructions. With 32 on-board 32-bit general-purpose registers, there is no need to access slow off-chip memory.

The V60/V70 feature an on-chip memory management unit with 4 gigabytes of demand-paged virtual memory space, and 4 levels of memory protection for multi-tasking and multi-user environments.

The V60/V70 instruction set is ideal for high-level languages and OS support (UNIX™ V and proprietary realtime OS). There are 21 addressing modes, 273 instructions, and an emulation mode for 16-bit V20/V30 software.

UNIX: trademark of AT&T Bell Laboratories.

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NUMBER 136

COMING SOON: 1.3/1.55μ DFB LASER DIODES.

Dispersion has always been a major obstacle in long-distance, high-speed lightwave communications. With conventional laser diodes emitting multiple spectrums, pulses deteriorate by dispersion after long travel through the fiber. This in turn limits repeater span to 20–30km and capacity to 400–560Mbps for the prevalent 1.3μ fiber optic systems.

NEC has overcome this obstacle with newly-developed distributed feedback (DFB) laser diodes for 1.3μ and 1.55μ fiber optic transmission systems. They feature a stable single longitudinal mode operation, high efficiency and high output power. The new DFB laser diodes are expected to expand repeater span to 80–100km for 1.3μ system or 100–200km for 1.55μ system.

NEC's new DFB laser diodes inherit the renowned double channel planar-buried heterostructure (DC-PBH) and have a diffraction grating in the optical guide region to produce a single wavelength. Output powers are rated 8mw for the 1.3μ NDL5600 and 5mw for the 1.55μ NDL5650. They come in the TO-5 package with an integral monitor photo diode or chip-on-carrier configurations.

As matching light-receiving devices, NEC has planar type InGaAs avalanche photo diodes. They have a selective guard ring construction to achieve high sensitivity and excellent reliability.

NEW INTELLIGENT BUILDING COMPLEX AT VANCOUVER.

The intelligent building is an idea whose time has come. As the perfect nestling for office workers in the Information Age, it centers on an advanced information management system which provides simultaneous voice, data and image services to tenants at less cost while it controls the entire building environment efficiently.

The World Trade Centre/Pan-Pacific Vancouver Hotel recently opened is just such an installation. NEC's NEAX 2400 Information Management System (IMS) allows tenants to utilize enhanced telephone/facsimile services including least-cost routing, message center and voice mail services, and computer terminal connection via a multifunction digital telephone set. The NEAX 2400 IMS also offers sophisticated services to hotel guests.

NEC's Intelligent Building Systems, based on our unique C&C (integrated computer and communications) technology, are the most advanced and comprehensive available today. As the core of this system, the modular NEAX 2400 IMS can expand to 255 tenant partitions. It supports more than a hundred advanced features including a protocol converter to allow communication with most popular host computers.

NEC also supplies comprehensive component equipment including multifunction digital telephones, information display pagers, high-speed facsimiles, business and personal computers, teleconferencing and CATV equipment and local distribution microwave links.

NEC's comprehensive systems breathe new life into the smart building concept, bringing costly services like teleconferencing within the reach of every business.

NEW HIGH-CAPACITY 64QAM DMR SERIES.

NEC's newest 800 Series high-capacity digital microwave radio (DMR) systems transmit two or three DS3 signals per RF carrier, utilizing 64-state quadrature amplitude modulation (64QAM) for effective use of radio spectrum.

Three systems meeting FCC standards are available: a 4GHz 90M-bit system providing 1,344 voice channels, and 6GHz and 11GHz 135M-bit systems for 2,016 voice channels.

The new systems incorporate the latest LSIs, hybrid and microwave ICs throughout to achieve compact design, lower power consumption and improved system reliability. Housed in a standard 19-inch rack, they require minimal cabling work for installation.

The advanced 800 Series is fully compatible with Bell's facility maintenance and administration system.

NEC

INTERNATIONAL NEWSLETTER

THE JAPANESE ARE PUSHING WORK ON BIGGER LCD PANELS . . .

The race is on in Japan to develop what promises to be the next generation of full-color displays for TV receivers and personal computers: large active-matrix color liquid-crystal displays. One maker of production equipment, Nikon, is said to have shipped about 20 steppers capable of making masks up to 400 mm on a side. Steppers with a working area many times larger than that for direct write-on-chip semiconductor lithography are necessary for volume production of the larger active-LCD matrixes. The largest active-matrix color display so far is Seiko Instruments and Electronics Ltd.'s 14-in. panel with a resolution of 640 by 400 dots. Among other large units are a 12.5-in. display from Matsushita, a 10-incher from Mitsubishi, a 7.2-in. one from Hoshiden Electronics Co., and a 6.3-in. one from Hitachi. □

. . . INCLUDING SUPERTWISTED BIREFRINGENT MODELS

Another type of liquid-crystal display—the supertwisted birefringent-effect reflective display—is moving toward year-end production. The major advantage of these monochrome panels is their contrast, typically with a ratio of more than 10, over a wide viewing angle. That compares with 3 or 4, with a narrow viewing angle, for the twisted nematic LCD screens now available for laptop computers and similar applications. At two recent shows in Tokyo, Japan Display '86 and the Japan Electronics Show, supertwisted panels measuring 10 in. diagonally with a resolution of 640 by 200 dots and high contrast ratio were shown by Asahi Glass Electronic Products R&D Center, Konishiroku Photo Industry, and Seiko Instruments and Electronics. Also on display were LCD panels fabricated in ferroelectric chiral smectic C LCD technology, which needs no refresh until information is updated. However, observers at the shows said that panels using ferroelectric LCD technology are about two years from production. □

MONOLITHIC MULTIPLEXER AIMS FOR RECORD BIT RATE

West German engineers are on the track toward a record bit rate for monolithic multiplexer-demultiplexer ICs. Researchers at the Institute for Electronics at the Ruhr-University in Bochum say they have developed a time-division multiplexer and signal-regenerating demultiplexer IC that operates at up to 6 Gb/s. They say they could hit a record 10 Gb/s by switching from a standard 2-μm bipolar technology to a 1-μm self-aligned polysilicon process. By way of comparison, AT&T Bell Laboratories reported at the 1986 International Solid State Circuits Conference on a 1-μm n-MOS chip that operates at 3 Gb/s. Hitachi Ltd. has reported a 6-Gb/s bipolar multiplexer-demultiplexer IC These ICs could boost transmission rates in optical-fiber systems. □

SPAIN SEES LITTLE PROGRESS IN DRIVE FOR COMPUTER SELF-SUFFICIENCY

Spain is still too dependent on foreign manufacturers for data-processing equipment and services, says the government's Department of Electronics and Data Processing. However, some of the objectives of the national plan to gain self-sufficiency have been achieved, the department says. For example, national production of computer equipment totaled $610 million, up 32% from 1984. On the down side, although investment in the industry grew a moderate 15% to $95 million, nearly 80% of that represents IBM España's investments in its plant in Pobla de Valbona, Valencia; Nixdorf España accounted for another 14%. The industry's total export volume rose 36% to $574 million—but nearly 90% of the total came from IBM. Contributing to the dismal picture, Spain's trade deficit in data processing rose from $978 million in 1984 to $1.2 billion in 1985. □

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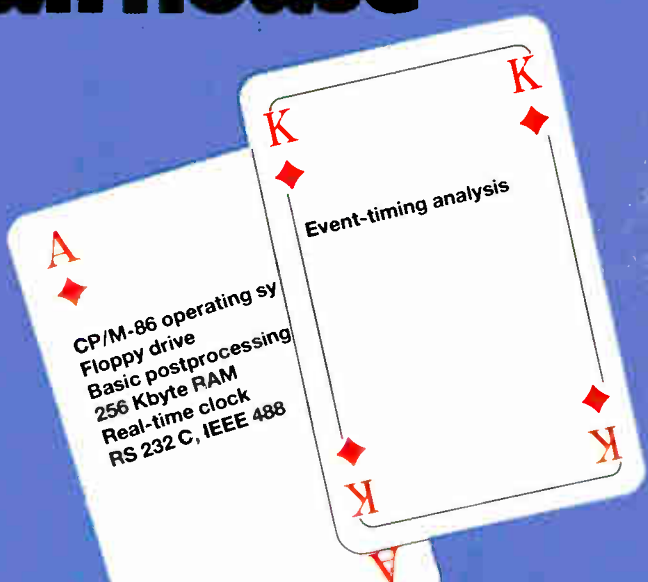

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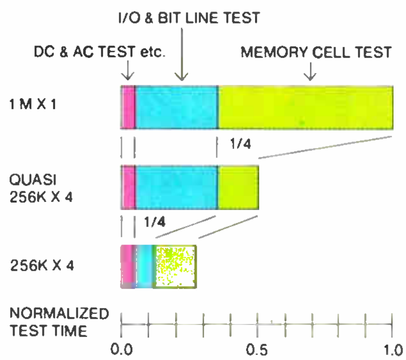

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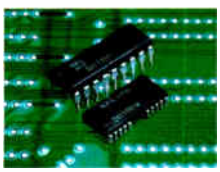

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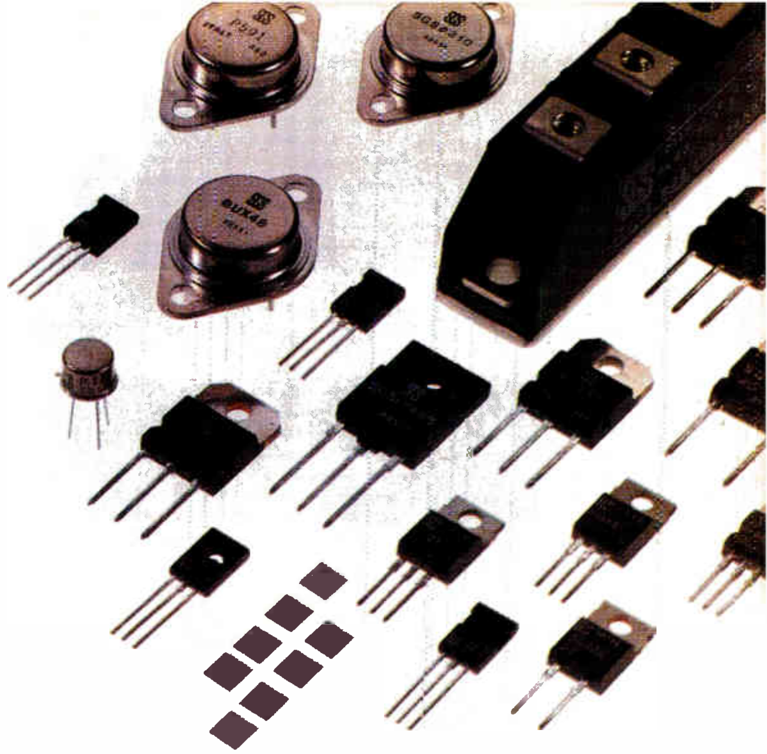

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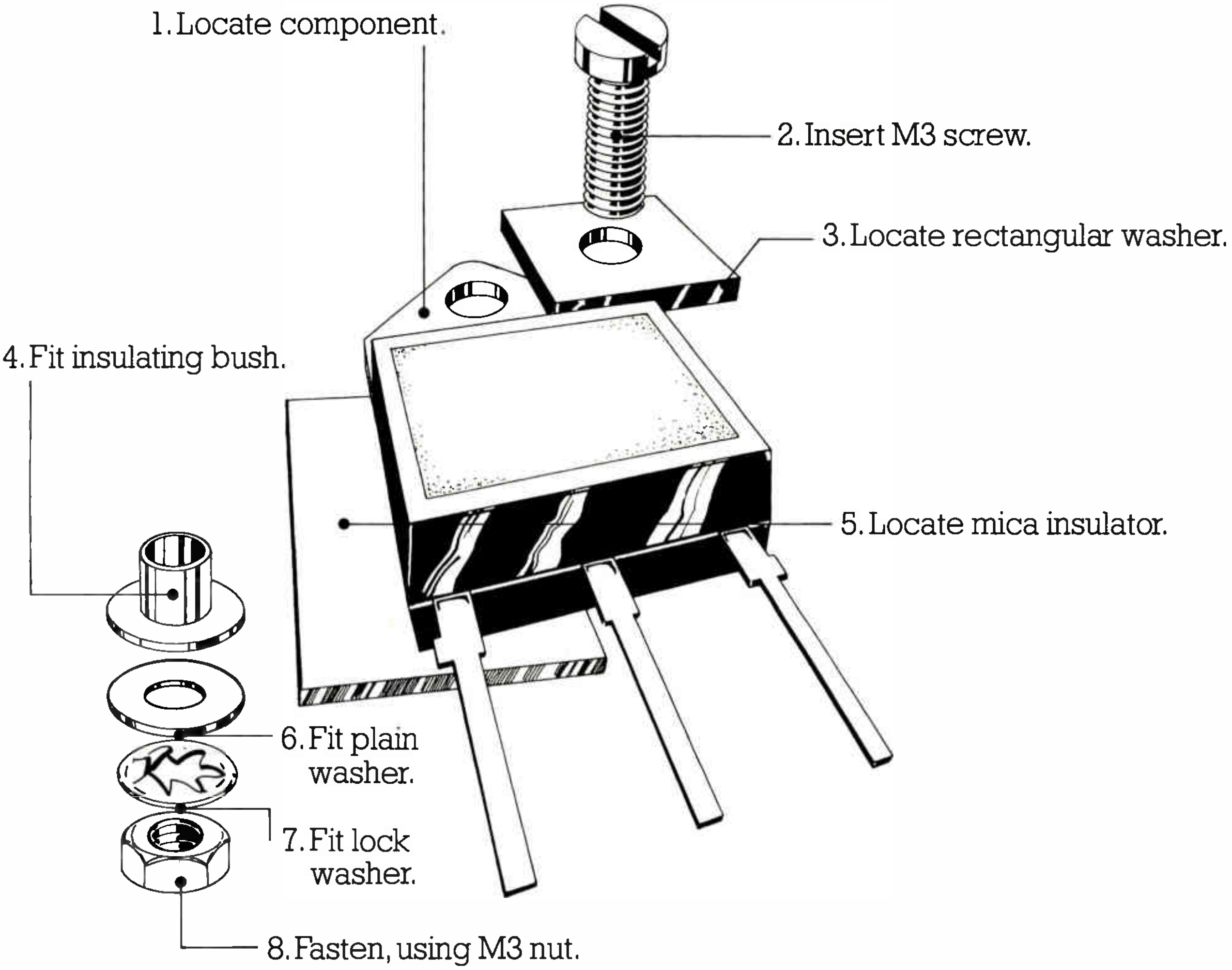

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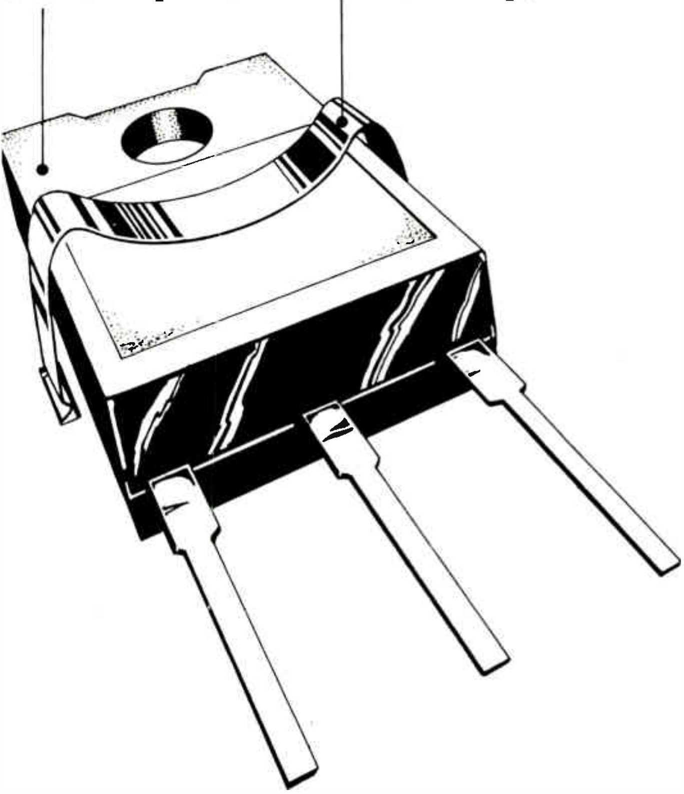

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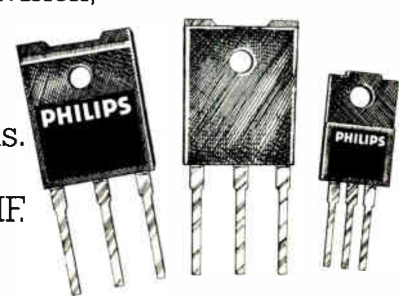

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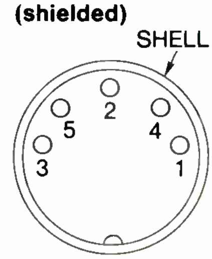
Connector Pin Assignment

Pin number	Signal
1	CLOCK
2	DATA
3	N.C
4	GROUND (SG)
5	+5Vdc
SHELL	GROUND (FG)

DIN Connector (shielded)



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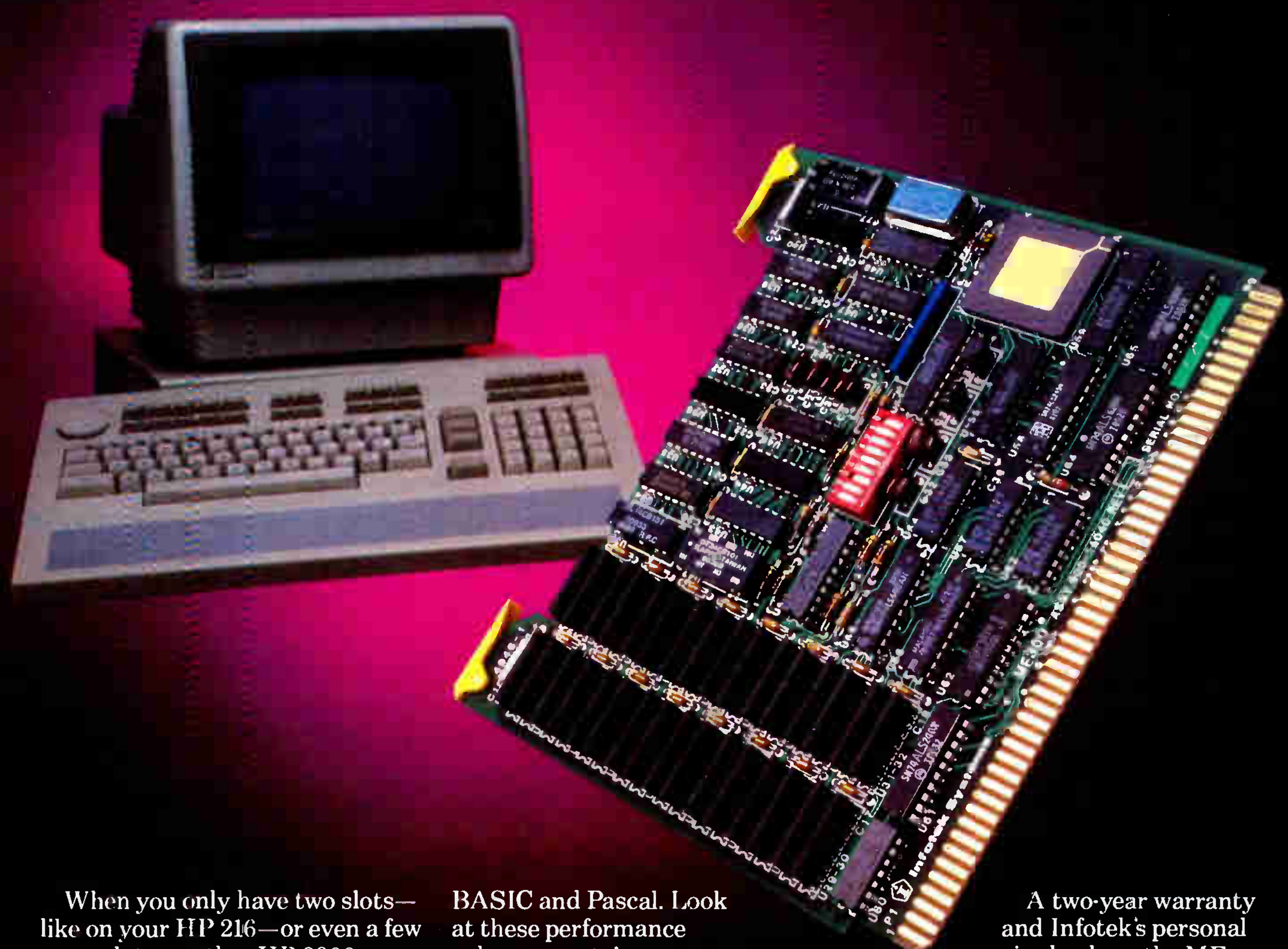

When you only have two slots—like on your HP 216—or even a few more slots as other HP 9000 computers do, you have to put the most capability in the least possible space or you may be limiting your computer's life!

So, now you can have memory—one, two or a full four megabytes—plus an advanced floating point processor on a single card with the new MF 300 Series from Infotek.

The MF 300 Series incorporates a powerful floating point processor (based on the Motorola 68881 processor) which significantly increases the speed of transcendental functions as well as arithmetic operations for both BASIC and Pascal. Look at these performance enhancements!

Compiled BASIC

Statement	Computer	Without MF	With MF	Ratio
X=Y*Z	216	259	50	5.2
	310	161	37	4.2
X=SQRT(Y)	216	2,117	38	56
	310	1,333	30	44
X=SIN(Y)	216	4,326	64	68
	310	2,746	50	55

The same performance (without the memory) is available in the new FP 881 floating point processor. Or you can choose the Infotek FP 210 floating point processor for BASIC and Pascal based on the National 32081.

A two-year warranty and Infotek's personal service back up the MF 300 Series. So give new life to your HP. Call today for full information and ask to be put on the mailing list for our newsletter. (800) 227-0218, in California (800) 523-1682 or (714) 956-9300, 1400 North Baxter Street, Anaheim, California 92806-1201, TELEX 182283.

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Circle 51 on reader service card

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How we know the exact needs of high-quality automated board production? Well, a fair share of the world's automatic mounting equipment—the Avimount series—comes from TDK.

Product name		Type	Shape	Dimensions L (mm)	W (mm)	T (mm)	Electrical Characteristics
Multilayer Ceramic Chip Capacitor		C1508		1.5	0.8	1.0	C: 0.5～470pF, 100～22,000pF
		C2012		2.0	1.25	0.6	C: 0.5～1,800pF
						0.85	C: 470～100,000pF
						1.25	
		C3216		3.2	1.6	0.6	C: 0.5～270pF
						0.85	C: 470～220,000pF
						1.1	
		C3225		3.2	2.5	<1.9	C: 750～8,200pF, 56,000～470,000pF
		C4532		4.5	3.2	<1.9	C: 2,400～18,000pF, 180,000pF～1μF
		C5650		5.6	5.0	<1.9	C: 5,100～33,000pF, 270,000pF～1.5μF
Multilayer Ceramic Chip Capacitor (High Frequency, Los Loss)		FC1414		1.4	1.4	1.6	C: 0.5～100pF, 150～3,300pF
		FC2828		2.8	2.8	2.8	C: 0.5～1,000pF, 470～22,000pF
		FR1414		1.4	1.4	1.6	C: 0.5～100pF, 150～3,300pF
		FR2828		2.8	2.8	2.8	C: 0.5～1,000pF, 470～22,000pF
Wound Chip Inductor		NL322522		3.2	2.5	2.2	L: 0.01～220μH
		NL453232		4.5	3.2	3.2	L: 1.0～1,000μH
		NLF453232		4.5	3.2	3.2	L: 1.0～1,000μH
Multilayer Chip Inductor		MLF321606		3.2	1.6	0.6	L:0.047～220μH
		MLF321611		3.2	1.6	1.1	
		MLF322511		3.2	2.5	1.1	
		MLF322518		3.2	2.5	1.8	
		MLF322525		3.2	2.5	2.5	
Multilayer Chip Transformer		MTT4532		4.5	3.2	2.8 max.	L: 10～200μH
Multilayer Chip IFT		MIA4532		4.5	3.2	2.8	F: 455, 459, 464kHz
		MIF4532		4.5	3.2	2.2	F: 10.7MHz
Multilayer Chip LC Trap		MXT4532		4.5	3.2	2.8 max.	F: fo ±2%
Multilayer Chip LC Filter	HPF (Tuner)	MXF4532H		4.5	3.2	2.8 max.	Electrical characteristics are representative, please specify value when ordering.
	BPF (FM radio)	MXF4532B		4.5	3.2	2.8 max.	
	BPF (VCR)	MXB5050B		5.0	5.0	2.8 max.	
	LPF (VCR)	MXB5050L		5.0	5.0	2.8 max.	
	Equalizer (VCR)	MXB5050E		5.0	5.0	2.8 max.	
	Delay Line (VCR)	MXB50500		5.0	5.0	2.8 max.	
Multilayer Chip Capacitor Network		MCN7575		7.5	7.5	0.9	C: 1～1,000pF (TC:CH) (10 capacitors) C: 10～1,000pF (TC:SL) (10 capacitors)
Ferrite Chip Beads		CB201209		2.0	1.25	0.9	Zo: 7, 10, 11Ω
		CB321611		3.2	1.6	1.1	Zo: 19, 26, 31Ω
		CB322513		3.2	2.5	1.3	Zo: 31, 52, 60Ω
		CB453215		4.5	3.2	1.5	Zo: 70, 120, 125Ω
SM Active Delay Line		FDL		12.0	9.5	5.6	Delay time: 20～250 nsec.
SM Transformer/ Inductor		EE5		7.4	5.3	4.75	Electrical characteristics are representative, please specify value when ordering.
		ER9.5		11.5	9.5	6.3	
		ER11		12.5	11.0	6.3	
		T2		7.0	5.0	2.2	
Step-up Inductor (Piezo Buzzer)		OL3.3×1.6		5.6	5.3	1.6	Inductance values are representative, please specify value when ordering.
		OL3.3×2.1		5.6	3.3	2.1	

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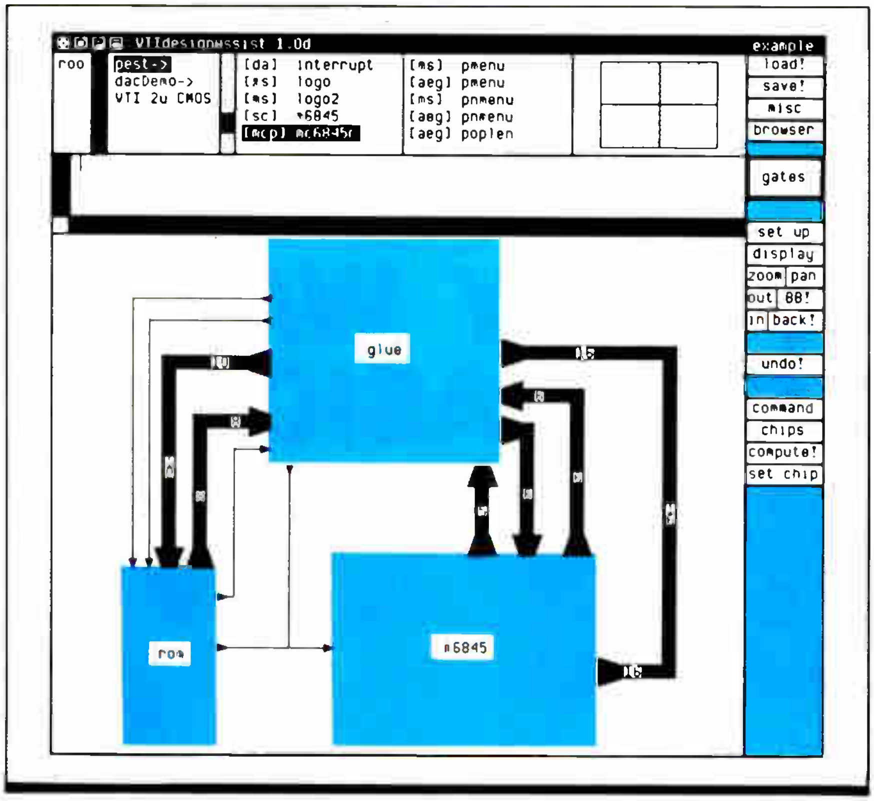
Circle 52 on reader service card

A NEW, EASY WAY TO DESIGN ASICs

A powerful new software tool is poised to simplify and speed up the design of application-specific integrated circuits. The Design Assistant from VLSI Technology Inc. provides the equivalent of the "what-if" analysis an accountant gets with an electronic spreadsheet. It can quickly evaluate all the alternatives to consider in designing an ASIC. With it, both experienced and novice ASIC designers can examine different implementations early in the design cycle, before the project gets under way and costs begin to mount. The Design Assistant "aids the ASIC designer in making cost and feasibility tradeoffs



WINDOW ENTRY. The Design Assistant allows the designer to enter and link the major blocks of the design in a graphical window.

between the various design implementations: gate arrays, standard cells, silicon compilations, or full-custom," says Douglas Fairbairn, vice president of design technology at the San Jose, Calif., company. "It provides feedback on chip size and power, packaging alternatives, relative cost, and performance."

Also, a designer must choose whether to implement the entire design on one chip or split it into several chips. He must consider cost, any special packaging requirements, and the amount of time he has to complete the design before the market window for his product closes.

Using the designer's general description of the planned chip, the Design Assistant generates alternative floor plans and displays them on a work-station screen

Until now, this kind of analysis has been a lengthy, complex process that requires the expertise of a design center engineer. The purpose of the Design Assistant is to provide a quick, easy route to developing a product from the basic take-off point—a tool for nonexperts who need expert results.

"The tool automatically generates floor-plan alternatives from a general chip description and displays them on a work-station CRT screen," Fairbairn says. "It enables the designer to make basic system-partitioning tradeoffs early in the design cycle."

Scheduled for general release in the second quarter of 1987, the tool runs on an Apollo DN3000 work station. "The Design Assistant is implemented as a graphical window that allows the designer to enter and link the major blocks of his design, as with a simple schematic editor," says Paul McLellan, manager of VLSI software development-Europe and the developer of the Design Assistant. "However, it is much less restrictive than an editor. For example, it can connect blocks simply by drawing a signal [line] to the block, and no previously existing connector is required on the block."

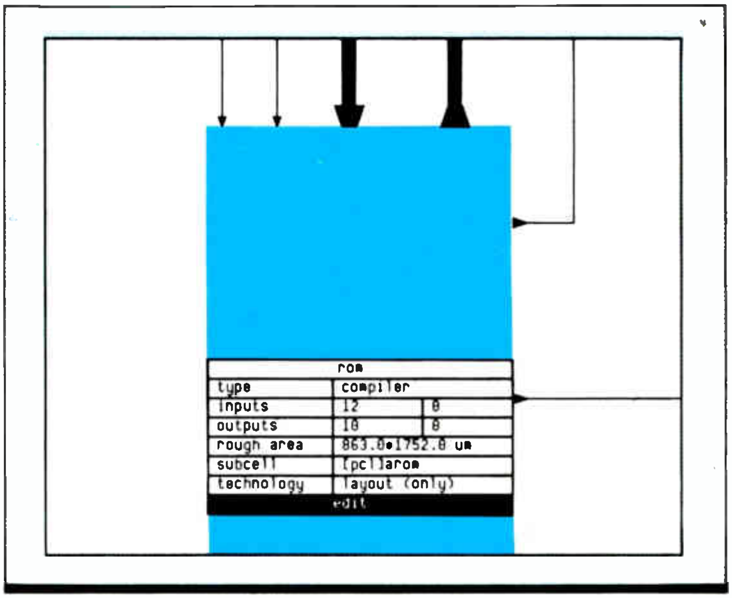
The top part of the screen is patterned on the standard interface of all VLSI Technology design tools. It contains a browser, which provides a graphical interface to the data manager that underlies all the tools (Fig. 1). Below this part is a text area (shown blank in this example), which provides a record of the session; the information shown here can be printed or saved in a file. Below the text area is a window that contains the design, in this case a CRT controller consisting of a 6845 CRT controller chip, a ROM, and 900 gates of glue logic.

Using the Design Assistant, the operator can enter and specify blocks in different levels of detail: a netlist, a gate count, a list of cells involved, a schematic, a laid-out megacell (a fully laid-out circuit), or an estimator or predictor of the amount of area a silicon compiler circuit will take up on the final chip. Each block displays a form (Fig. 2) containing data about the block, some of which can be altered. In the rows labelled "inputs" and "outputs," the middle column is the number of on-chip connections and the right-hand column is the number of off-chip connections. Such signals can also be specified by drawing wires or buses to explicit symbols external to the design. In a single-chip design, all three of the blocks of CRT controller are assigned to a single chip; if the design is to contain multiple chips, the blocks are assigned to the individual chips.

"For any assignment of blocks to chips, the Design Assistant estimates power dissipation, possible packages for the die, and die size for each chip," McLellan explains. "Thereafter, if the designer partitions the design differently, the software changes estimates accordingly." For example, putting one of three blocks from a single-chip design into a separate chip changes intrachip signals into interchip signals and thus alters the input/output pad requirements for the chips in the new partition. The Design Assistant software tool automatically changes pads on the CRT screen for the new design.

ASKING 'WHAT IF' QUESTIONS

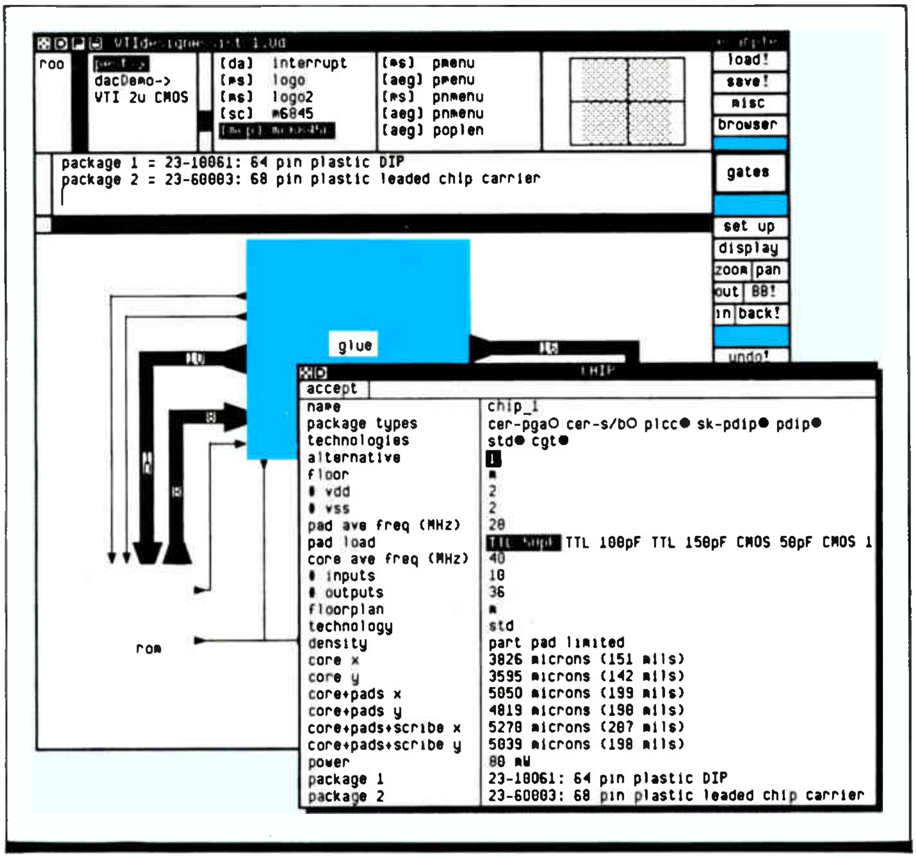
In performing its analysis, the Design Assistant takes into account obvious factors such as the area of the cells, compilers, and gate-array macros. For gate arrays, the Design Assistant uses data about the size of macros and the sizes of the available gate-array bases. It also estimates standard-cell and interblock routing, as well as routing from the core to the pads. It automatically handles the choice of pad sets, depending on whether the design is core-limited—limited by the number of gates the array contains in its core—or pad-limited, that is, limited by the number of I/O pads the array can contain. It calculates the power dissipation from the average operating frequency of the core of a standard cell, gate array, or full-custom chip. In making a package choice, it considers the size of the die, the number of pins required, and the power dissipation of the chip.



DATA FORM. By zooming in on a block, the designer can read data concerning it, and alter it if he needs to.

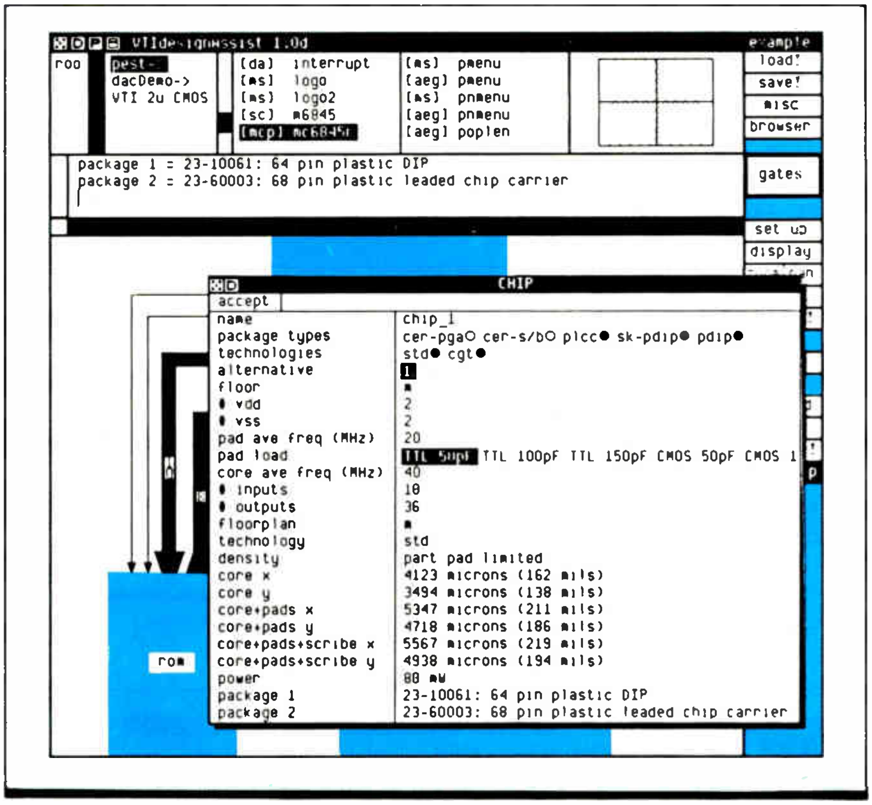
"Once the Design Assistant evaluates the design, it generally suggests several different possibilities for the chip," McLellan says. "Depending on the details of the block, several different floor plans [chips with various lengths, widths, aspect ratios, and the like] may be possible. An alternative with the smallest area may not always be the best choice, since the dimensions of the chip may be too rectangular to fit into the available standard packages." In addition, certain designs preclude gate arrays as an alternative—for example, designs containing on-board ROM and random-access memory.

The designer may ask the tool "what-if" questions. He may, for example, ask for the parameters on a single-chip implementation of his design, and the Design Assistant responds with a property sheet, which overlays the window (Fig. 3). In the sheet, the first few lines are specified by the designer: "name" and "package types." The designer in this case has ruled out ceramic pin-grid arrays and ceramic side-brazed packages as choices by clicking on the first two dots on the second line. The remaining lines are produced by the Design Assistant.



OPTIONS. When the designer wishes to evaluate alternatives, the Design Assistant software can display a property sheet overlaying the window.

In this instance, the Design Assistant's analysis estimates that the single-chip design requires a 207-by-198-mil chip (about 5.3 mm by 5.0 mm), and it determines that the best packages in each of two possible package families are 23-10061 and the 23-60003 plastic leaded chip carrier. There is no feasible choice in the third package family: skinny plastic dual-in-line packages. And because the design example contains a ROM, it



CHECKING ALTERNATIVES. The designer may want to partition the design differently to see what effect doubling the ROM size s on overall chip area.

When the designer settles on an implementation, the Design Assistant writes schematic templates for each chip and for each block that is not predefined. This eliminates the errors that frequently occur when entering the schematic: not making all the connections between components of a design, reversing connections, and so on. The Design Assistant also places the I/O pads with the appropriate signals, thereby eliminating another common source of operator-induced errors.

In order to carry out its functions, the Design Assistant has two major components: an analysis program and a technology file that contains all available information needed to evaluate the design and calculate alternatives. "The analysis part of the design comprises two parts," says McLellan. "The first partitions the design into chips as specified by the designer." During the analysis, the software determines whether each signal is within a single chip, or if I/O pads are required to allow the signal to move between one or more chips in a multiple-chip design.

Also in this first part of the analysis, the designer enters data on the number of supply voltage pads, operating frequency of the circuit, and so on. At the conclusion, the Design Assistant has compiled a list of all the information known about a single chip or about each chip in a multiple-chip design. This data is then passed to the second part of the analysis.

"In the second part of the analysis, the software compares the circuit-design requirements with available technologies in which to implement the circuit," McLellan explains. The technology file, which contains this information, is loaded when the Design Assistant is initiated. It contains two types of information.

The first type of information includes data about standard cells, gate-array macros (hard layout of standard logic functions, inverters, and AND and OR gates), gate-array bases, soft macros (complex functions such as an adder, which is built from basic gates and flip-flops), available packages—all the information a human expert would need in order to evaluate the range of alternatives for implementing a design.

For example, the data for a set of standard cells describes the type of devices and their height. Thereafter, the file lists all the standard cells in the set: "gate," "ad01d1" (1-bit full adder), "ad02d1" (2-bit full adder), and so on. Each standard cell in the set is described. For example, a 1-bit full adder is 150 μm long, consumes 60.6 μW of power for every 1 MHz of operating frequency, contains five I/O terminals (four in-

can only be implemented as a standard cell, not as a gate array, if it is to be contained on a single chip.

The designer can work with this implementation, partitioning his design differently to see if he can achieve a better solution. He may, for example, decide to make the ROM twice as large and change its aspect ratio by pulling up the ROM parameter sheet and altering the values. This would increase the chip size (Fig. 4) to 219 by 194 mils (5.6 mm by 4.9 mm).

LOOKING AT ALTERNATIVES

The designer might choose to put the glue logic of the CRT controller design into a gate array in order to connect standard chips. To indicate this to the Design Assistant, he makes the two blocks off-chip elements. The Design Assistant then performs the evaluation. In this case, there are too many I/O pads in the resulting alternatives.

The gate array alternative in the CRT controller example will show that the number of pads required forces the use of a 6,000-gate base—in which only 23% of the gates are used. Another alternative, the standard-cell approach, shows that the glue-logic chip would be as large as the original chip containing the ROM and the CRT controller—211 by 211 mils (5.4 mm on a side). In addition, the chip would be so pad-limited that only 43% of the gates enclosed in the core would be used for cells or routing.

put, one output), and is implemented with 10 gates.

Another part of the technology file could contain a description of the set of soft macros available to the designer. The soft macros are the equivalent of the popular 74LS small- and medium-scale-integrated family of TTL logic functions: DIPs containing six inverters or four two-input NAND gates, etc. This logic family has its equivalent in soft macros available to the designer building gate arrays. For the gate-array vendor, having a library of soft macros equivalent to a popular logic family means that designers can take their pc-board designs and easily put them into a gate array. In a typical set of soft macros, "ls00"—a two-input NAND gate with four inputs and one output—is the logic equivalent of a 74LS00 SSI device.

The second type of information in the technology file is procedures (algorithms) for estimating routing, determining which pad sets to use, selecting packages, estimating power dissipation, assessing sizes of various floor plans, and ruling out impractical implementations such as odd-shaped dice. For example, a procedure for calculating the size of a die takes into account that there are two sets of pads. One is used for core-limited designs, the other for pad-limited designs. The first is square; the second is rectangular, so more can be placed side by side around the perimeter of a chip. A design may be partially pad-limited with the square pads but core-limited with rectangular pads.

A choice between core-limited and pad-limited pad sets is made based on the number of pads, the estimated core size, and the size of the pad ring. The width of the scribe line (the line made by the diamond saw cutting the chips from the wafer) is added to calculate the overall die size. Another procedure calculates the power dissipation of the chip. It determines the dc power dissipated, if any, and combines this with the ac power based on the average operating frequencies of the core and the average frequency for the pads, together with the pad loading. The procedure uses a figure of merit of 1 mW for each 1 MHz of operating frequency.

With the Design Assistant, a design can be evaluated in a day or so; it might then be engineered in a month or two. In the example shown here, a designer would have to perform a schematic capture of only the glue logic, because the ROM and 6845 exist as models. They are automatically entered into the VLSI Technology data base, ready to be passed into the foundry's schematic-capture tool.

After partitioning the design into the specified chips, the Design Assistant analyzes it in terms of the technologies that are available to implement it

Once the remainder of the design has been entered, the entire circuit can be simulated and debugged. Next, the foundry places and routes the circuit, and the results are given back to the company for final verification. If no errors are detected at this time, the standard-cell parts could be produced in six to eight weeks, and the complete design could be in production in six to eight months—half the time it might take to get the new chip to market without this kind of automatic, easy-to-use evaluation tool. □

PUTTING DESIGN EVALUATIONS IN THE FAST LANE

The customer meeting put a recurring problem into sharp focus for Douglas Fairbairn, a founder of VLSI Technology Inc. and vice president of design technology. "To this meeting, each customer would send a group of experienced IC designers for a consultation with our IC layout experts," he says. "In the room were all these experienced designers, and they were all trying to do a design evaluation." The evaluation would be successful, but it took time—in some cases hours or days—and a lot of costly collective engineering expertise.

Fairburn realized that VLSI Technology's customers had to go through this process for every ASIC design they sent to the foundry. Moreover, the problem was worse for a customer who was a systems designer inexperienced in implementing an integrated circuit. For example, such a designer had no feel for the size of different circuit components, so it was even harder for him to make tradeoffs. And lately, the success or failure of a product can hinge on making the right initial implementation choices.


FAIRBAIRN

Fairbairn was the one who defined the Design Assistant analysis tool, seeking a product that would automatically perform all the evaluations that several IC engineers would laboriously produce with calculators and paper. But it fell to Paul McLellan, a software engineer, to make the idea work.

Developing the Design Assistant was to be a quick-turnaround project. The concept was formed in January, and McLellan was writing code by March.


McLELLAN

"We plan to start using the Design Assistant in our design centers to determine how well it serves the customer's needs," says McLellan. "We're looking, first, to see that the tool actually serves the designer's needs, and we're looking for additional features that can be added to the product that will make it more applicable to a wider range of the designer's needs."

Now that the Design Assistant is on the way to its launch, its developer has moved on in VLSI Technology. "In January of this year, I became the manager of VLSI software development in Europe," says McLellan. He moves to France this month.

The road to the future is pa

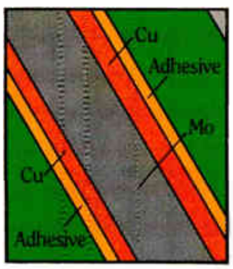
DENSER PACKAGING.

Surface-mounted leadless ceramic chip carriers offer tremendous potential.

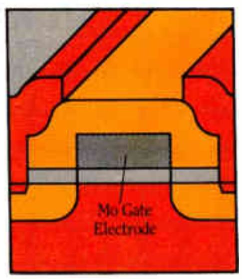
But because of the severe thermal expansion mismatch between ceramic chip carriers and traditional PC board materials, solder joints can fail after thermal cycling. Plus, the higher packaging density generates even more heat, causing further problems for traditional PC board materials.

The best way to take the heat off: incorporate a copper-clad molybdenum metal core in the PC board. One, this unique material solves the problem of thermal mismatch with its ultra-low coefficient of expansion. Two, it serves as an integral heat sink. And, three, it significantly increases the rigidity of the board, preventing solder-joint failure due to flexing, warping or twisting.

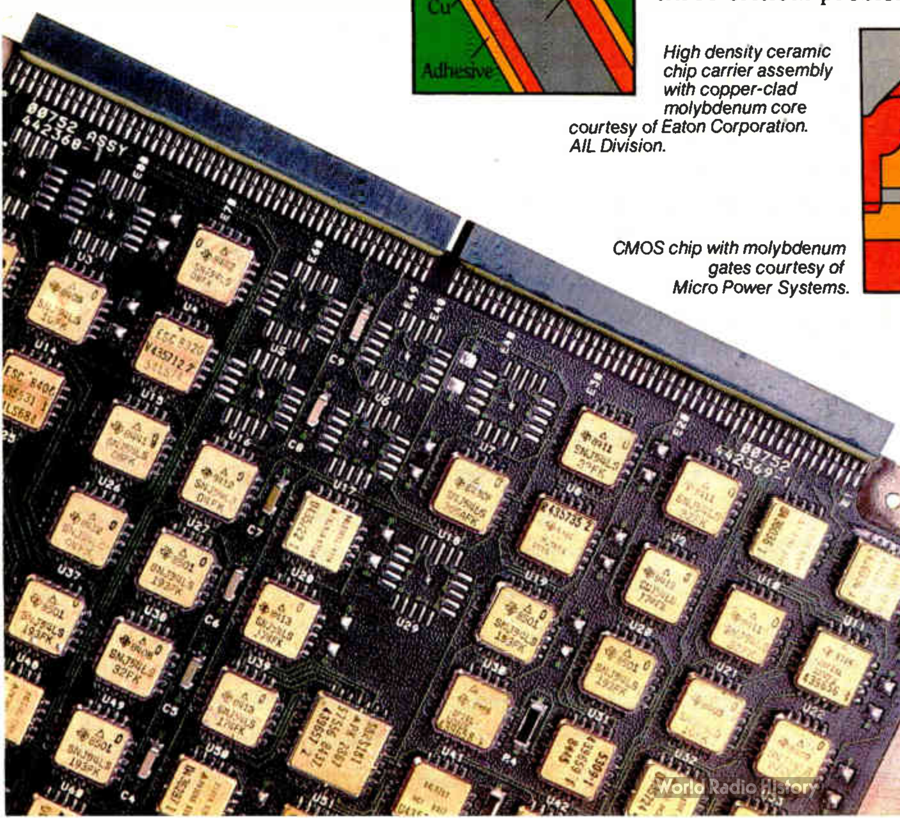
In fact, copper-clad molybdenum is superior to any other laminated metal approach to these three critical problems.



High density ceramic chip carrier assembly with copper-clad molybdenum core courtesy of Eaton Corporation. AIL Division.



CMOS chip with molybdenum gates courtesy of Micro Power Systems.



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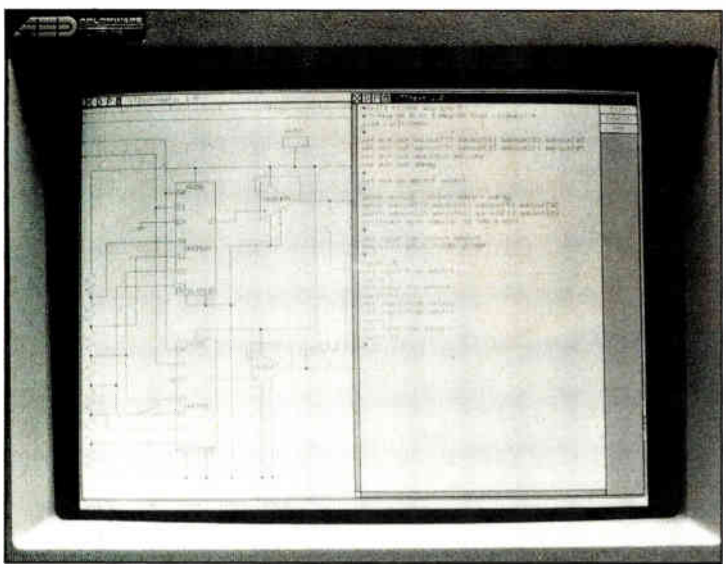
SIERRA'S NEW SIMULATOR SPEEDS UP ASIC DESIGN

Sierra Semiconductor combines behavioral models of its analog standard cells with a digital simulator to cut the time needed to check out analog-digital ASIC designs

Streamlined simulation of an application-specific integrated circuit that combines analog and digital components is the goal of a new package from Sierra Semiconductor Corp. The San Jose, Calif., company has put together a speedy combination of a modified digital simulator and a set of analog behavioral models stored in Sierra's standard cell library. The new combination can check out combined analog-digital IC designs in the same way as all-digital chip designs are now checked—with behavioral simulation, as opposed to the tedious device simulation done by the well-known Spice analog simulation tool.

At least half of all semicustom ASIC designs contain some analog circuits. Until now, incorporating analog circuitry in a digital standard-cell ASIC has been an expensive, time-consuming process requiring the services of a foundry that employs designers experienced in both analog and digital ASICs. Combining analog functions with digital standard cells has been difficult because the analog portion has had to be simulated separately from the digital part, and both must be debugged before they can be combined. Moreover, simulating complex analog circuits can take days or weeks of computer time. That's one reason Sierra's set of analog behavioral models (Fig. 1) was developed.



1. ALL TOGETHER. Sierra Semiconductor's analog behaviorial models simulate both analog and digital functions at the same time.

The other is to speed test-program generation. Just as behavioral simulators have helped automate test-program generation for digital ASICs, the Sierra tool set is designed to automate test-program generation for combined analog-digital ASICs. "Testing is a problem with analog ASICs, just as it was with digital ASICs before simulation," says Gary Allman, staff engineer at Sierra. "With logic simulation now commonplace, it takes a test engineer no more than half a day to convert a [logic] simulation into a test program. By contrast, it can take two to three months to generate a program to test an analog circuit.

"We're not to the point of producing analog test programs as quickly as digital test programs are created," he adds. "But including them in the overall digital simulation ensures that everything is hooked up correctly between the analog and digital circuits. It ensures that an inverter has not been left out of a design, or that an op amp's specifications have not been exceeded, or that a bus has not been hooked up opposite to the direction intended."

The Sierra product differs fundamentally from the Spice simulation program in that it uses a behavioral model to describe what a circuit does, rather than doing device-level modeling. Spice looks at an analog circuit, such as an operational amplifier, as a connected network of resistors and capacitors tied to a transistor. When a signal is applied to the base of the transistor, Spice models the behavior of each device in the circuit; the net result of each component working properly is that the correct output will appear from the circuit. However, the Spice simulator could easily miss an incorrect connection—it is not looking for proper connectivity; rather, it is checking only that the circuit functions properly as connected.

In contrast, the Sierra simulator views the op amp as an analog component that produces an output of certain amplitude and frequency in response to an input signal. The simulator does not look inside the op amp to see if its components are functioning correctly, but rather that the output is correct for the input and the operating conditions of the circuit—and that the op amp is correctly integrated into the design.

Both Spice and the Sierra simulator will produce the same result, but Spice will require far more in the way of computer resources, because it must model each of the devices in the design. And there is always the risk that Spice will fail to converge to a conclusion, in which case the designer will have to interpret the results of the simulation to find the kind of design errors the Sierra simulator can pinpoint quickly.

In converging to a conclusion, Spice makes a series of approximations as the program models each individual circuit component. But it can become hopelessly lost if the approximations do not become increasingly more accurate. There is a check in the program that indicates if it is successfully converging to an answer or not; if it is not, only a Spice expert can determine why, and how to rerun it so it does converge.

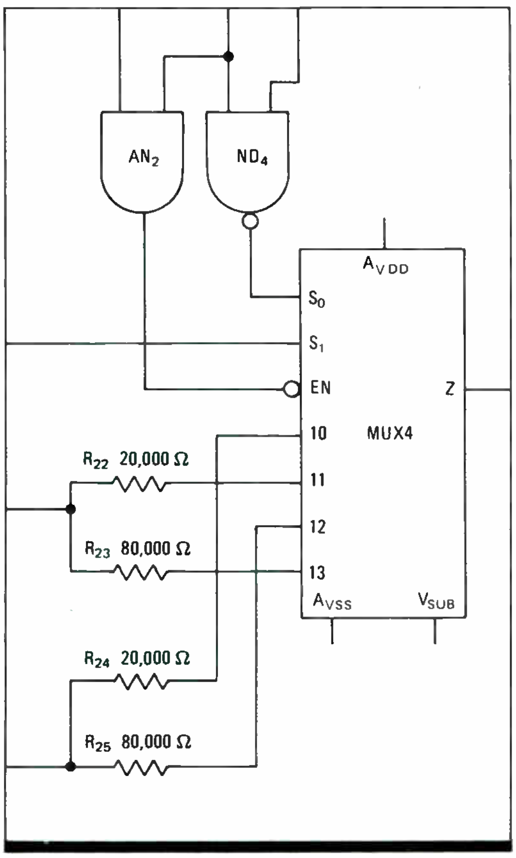
One approach to mixed analog-digital ASIC simulation makes use of Spice. Known as Splice, it allows the designer to designate certain parts of the circuit for logic simulation and other parts to be simulated with Spice—hence the amalgam of Splice, for both logic and Spice. However, like Spice, Splice simulation runs with large analog standard cells take a long time, because the simulator is checking the operation of every component of the circuit at different points in time.

HOW THE SIMULATOR WORKS

The Sierra simulator began life as a digital timing simulator licensed from VLSI Technology Inc. of San Jose. Sierra senior development engineer James Cadwell added extensions to it so that it could understand analog circuit characteristics in addition to 1s, 0s, and unknowns. A digital node needs to represent a 0, 1, unknown, or tristate condition. An analog node, by contrast, must possess qualities such as source resistance, load resistance, and continuous values of voltage and current.

In the Sierra standard-cell library, digital standard cells have only digital pins, and analog standard cells have both digital and analog pins. An analog multiplexer, for example, may have digital as well as analog inputs (Fig. 2).

The electrical model for the analog pin is like a Thevenin equivalent circuit. It has two sources—one being a median voltage, and the other uncertainty—on each of the lines coming into a node. At every analog node, there is a confluence of Thevenin sources, resulting in a voltage to any given pin relative to the other pins on the node.

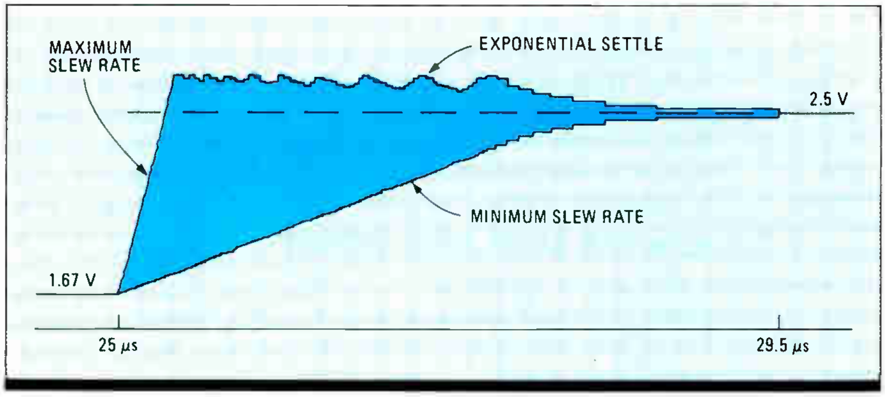


2. CHECKING BOTH. An analog multiplexer contains both analog and digital input pins, which the Sierra simulator can easily simulate concurrently.

In the simulator, a node-arbitration algorithm examines what is occurring at each pin, and a procedure can be called to describe the status of a node. It will activate the node arbitrator, which examines the influences on the node and comes up with a description of what is occurring on it.

The Thevenin-equivalent-model parameters are time-variable. They can be altered to respond to the conditions on the node to which the pin is attached. So the designer is not limited, say, to a model with a fixed resistance. "It can vary as a function of the voltage that exists on the terminal," says Caldwell. "Thus the effect of nonlinearity can be modeled."

Bidirectional behavior



3. ALL POSSIBILITIES. The Sierra simulator approximates an amplifier's ramp up in output voltage by considering all the ramp slopes the amp might experience.

can be modeled as well. That is, some analog terminals, such as those on resistors, can be neither inputs nor outputs, but instead can pass signals in both directions.

In addition, the simulator is able to represent a continuous degree of uncertainty to simulate the occurrence of transients. This enables the designer to take into consideration a range of circuit implementations that result from processing, temperature, and supply-voltage variations, all of which affect the exact signal coming out of a circuit.

The notion of continuous uncertainty can be illustrated by observing the change in output of an amplifier in response to an input (Fig. 3). The output will ramp upward, and the slope of the ramp will be determined by the slew rate of the amplifier. As the output nears its final value, it can overshoot and then oscillate around its final level; or, if the amplifier is heavily damped, the output can slope gently up to the final level.

The simulation does not attempt to model the amplifier's behavior exactly, since it has no way of knowing the exact behavior of the output waveform. Therefore it considers all the possible behaviors within the range of the maximum and minimum slew rates to determine if the circuit will operate in the final application.

Sierra is currently developing standard test packages for large standard cells, such as an analog-to-digital converter. Customers will always have certain unique implementations, though, so they will have to create their own test programs in order to test the unique parts of a circuit design. As the number of standard analog test programs included in the Sierra library grows, though, this need will likely diminish. □

TECHNOLOGY TO WATCH *is a regular feature of* Electronics *that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

HOW SIERRA BUILT ITS ANALOG-DIGITAL ASIC SIMULATOR

For most of the 13 years he has been an engineer, Thomas Tormey, the director of semicustom products for Sierra Semiconductor Inc., has been designing mixed analog and digital or pure analog ICs. Before joining Sierra, he was director of engineering operations at Zymos Inc., in Sunnyvale, Calif. "We had a small analog group there, and we attempted to do a number of mixed analog and digital circuits," Tormey explains. "But it was a time-consuming task, because no tools were available to help design the analog parts of these designs." In fact, he was attracted to Sierra because it had the right environment to develop these tools. "The company makes its living building ASICs with combined analog and digital components," he says.

THE A-D TEAM. Tormey (l.), Caldwell, and Allman (front) built Sierra's analog-digital simulator.

One of the two men Tormey enlisted to develop this simulator is Gary Allman, a staff engineer at Sierra, who is in charge of the analog cell library. "We had to create a library of behaviorial models that matched our analog standard cell library," says Allman, who graduated from the University of California at Berkeley at about the same time Tormey did.

"Having analog models reduces the amount of dumb errors that crop up in the course of a design," he adds. "In each model I've written are reasonableness checks that test if the voltage of a circuit element, such as an analog-to-digital converter, is out of range. If so, it tells the designer. The models also help in the test generation phase of a design cycle, since much of the simulation data can be used in generating the test. This also helps smooth the production of these chips by shortening the design cycle for mixed circuits."

To write the software that actually performs the combined analog and logic simulation, Tormey turned to James Caldwell, senior development engineer and a graduate of Massachusetts Institute of Technology. Starting with a simulator licensed from VLSI Technology Inc., Caldwell developed a body of appended code that understands voltage, current, and resistance. "So the designer is able to give the simulator a command such as 'set a voltage on terminal X,' and it knows what to do," Caldwell says. In addition, he says, "I had to add about 100 new functions and capabilities to the language so that it could be used to model analog functions."

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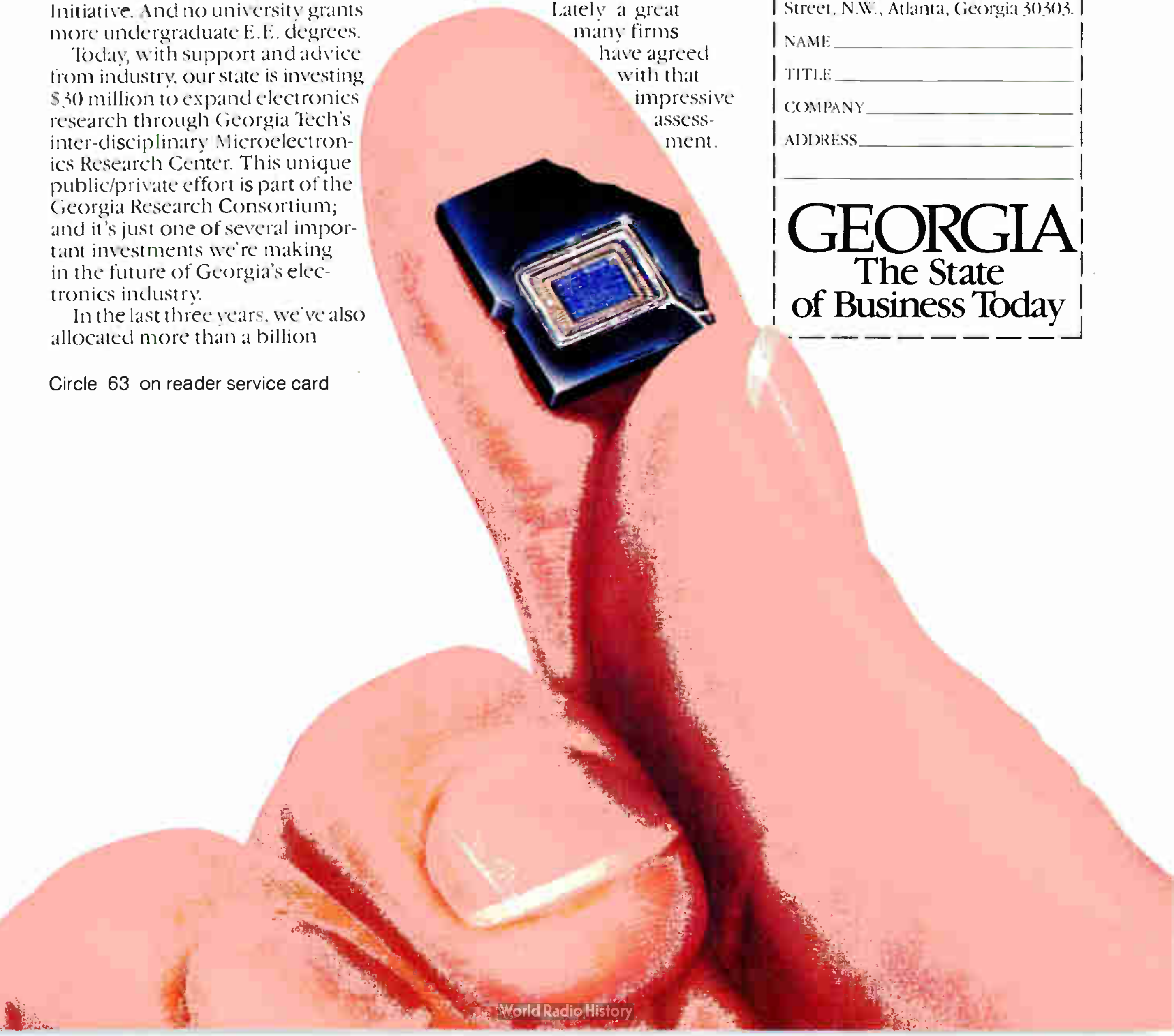


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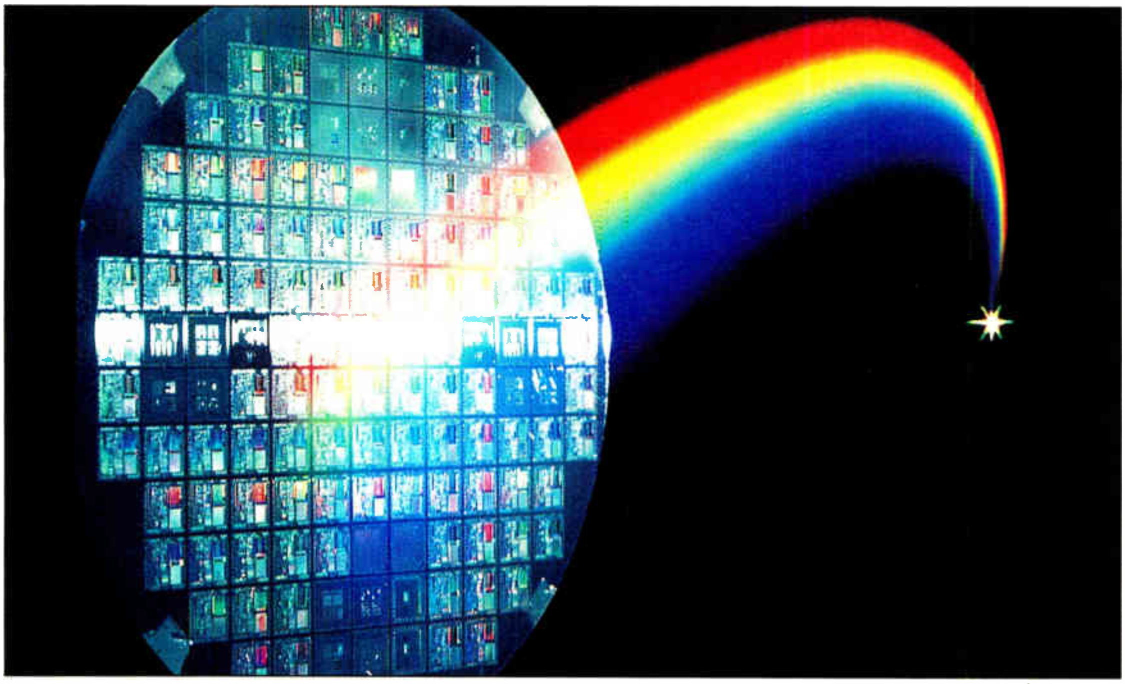
INSIDE TECHNOLOGY

TECHNOLOGY OUTLOOK



CONTENTS

While the outlook for the economy is still uncertain, technological progress shows no signs of slowing down in the year ahead. A steady stream of innovation is expected as the industry puts a wide range of technology to work, from GaAs VLSI and packaging to optical disks and parallel processing

COMPUTERS

New technologies, ranging from parallel processors to optical disks, will show up in computer systems next year, boosting performance and driving down prices

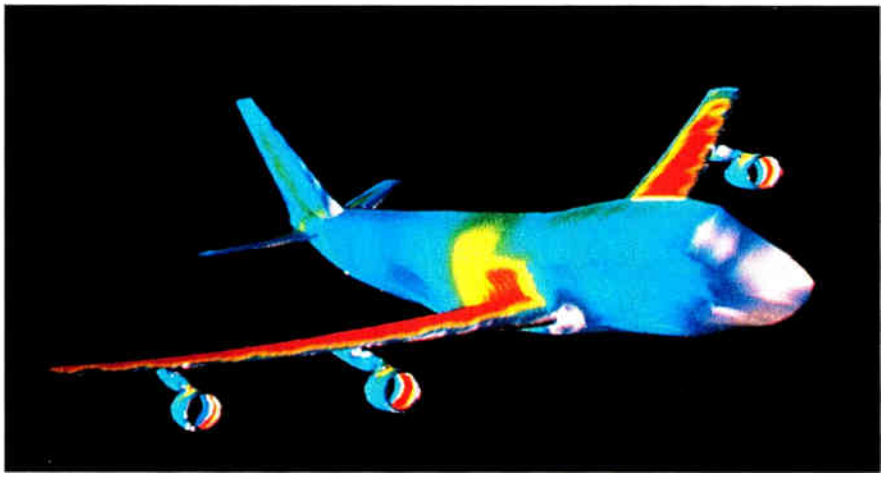
by Tom Manuel

Technology is flourishing and product development is on the move in the computer industry, despite a lingering weakness in sales. Industry observers are hoping, in fact, that a wave of new products—more powerful, less expensive, and easier to use—will spur an industry-wide turnaround during the coming year.

Innovations are being made on several fronts. In architecture, the trend toward scalable systems will continue, with more emphasis on parallel multiprocessor designs. Indeed, parallel computers are being heralded as a fundamental change in computer design, promising vastly increased performance for low cost.

New microprocessors, especially the advanced 32-bit engines, will likewise enhance price/performance ratios. Also contributing to the technological flowering are developments in reduced instruction-set computers (RISCs), the data-flow concept, extremely wide-word instructions, and the expanded use of special-purpose processors.

During the next year or two, attention will also focus on modeling and image processing in product design in a variety of industries, and on integrating personal computers, work stations, department or work-group computers, mainframes, and supercomputers. Developments in special-purpose work stations—graphics, engineering, scientific, electronic publishing, and so on—are coming fast and furious, while the next generation of super—or minisuper-computer—work stations will begin to emerge in 1987.



MODELED PLANE. Applications that combine modeling, image processing, and color graphics can simulate almost any product—even this Boeing 747, created at Princeton University.

Technical and scientific computing is a hot area of research and development, new products, and significant sales growth. The growth of sales in this segment, according to estimates by a variety of industry sources, is projected to be 30% to 35% or more annually for the next few years—the fastest growth in any segment of the computer industry. New high-end superminicomputers, minisupercomputers, and upgraded supercomputers are continually being unveiled. Most of the upcoming designs will be multiprocessor architectures, and many will be parallel computers that can be expanded to more than 10 central processing units.

In mass storage, optical devices—especially, in the short term, compact-disk read-only memories—will at last begin to make inroads. But developments in disk and tape drives and in bubble memories are keeping these magnetic technologies a fast-moving target. Computer display technology is no laggard, either. The next two to three years will see significant developments in flat-panel displays and continued enhancement of cathode-ray-tube devices.

EXPANDABLE ARCHITECTURES

Except for personal computers, customers are no longer interested in buying computers that can't be expanded but must be replaced. Users want scalable systems they can add to in stages without having to throw anything out. To meet this demand, many companies are turning to parallel multiprocessor designs—more than 40 manufacturers are building some kind of parallel processing system. "Parallel processing is the most fundamental change to occur in the computer industry to date," says Casey Powell, president of Sequent Computer Inc., the Beaverton, Ore., company that has been one of the pioneers in parallel systems.

Besides allowing systems to be expanded easily, architectures with multiple processing elements and large central memories built with very large-scale integrated circuitry provide far more power at a noticeably lower price. "Parallel computing will drive the industry—we are on the forefront of a major shift in the way we do computing," says Charlie Bishop, program manager for artificial intelligence at Intel Scientific Computers, Beaverton.

Not everyone agrees on just when this sea change will occur. "We do a lot of things in the lab that don't become products," says Tom West, vice president of the Systems Group at Data General Corp, Westboro, Mass. "Parallel machines fall into this category. Perhaps some day we will leverage these into the main-line products. Multiprocessor things will come along in a few years." In the meantime, the company will leverage its product line with advanced silicon circuits to run applications faster and cheaper.

Other trends in architecture are also making computing more affordable. Various RISC designs will be forthcoming, particularly in high-performance work stations. Data-flow architecture, another form of parallel computing, may leave the labs and appear in commercial systems. And a few companies are developing machines with very big instruction words. In allowing many operations in a single instruction, they represent yet another type of parallelism.

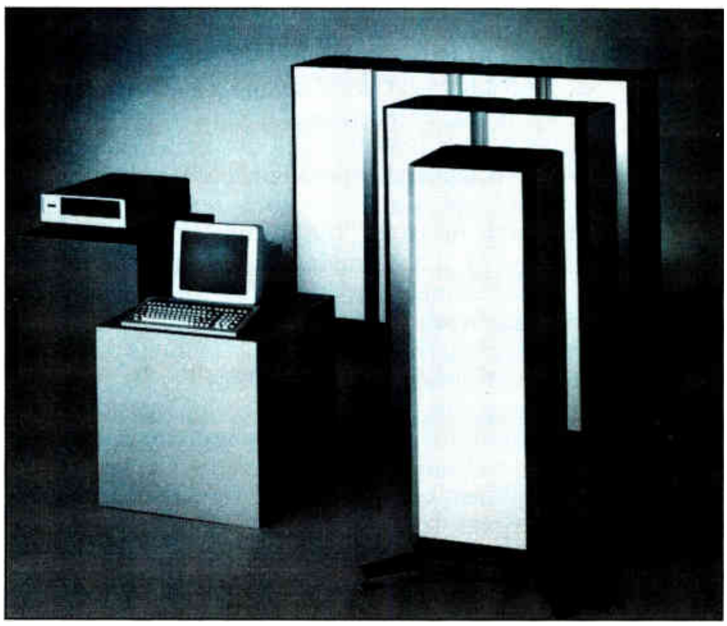
The 32-bit microprocessors that are just becoming available will be used in many of the new parallel computers, and in coming high-performance work stations. Powerful, but cost-effective microprocessors will make their own impact on computer design. In fact, says Gordon Reid, marketing manager for Intel Corp.'s development systems operations, Hillsboro, Ore., "32-bit applications are going to radically increase the numbers and kinds of problems solved by microprocessors—for example, real industrial applications, such as robotics, machine-tool control, and vision all require 32-bit processors."

Another continuing trend, the proliferation of special-purpose coprocessors, is being fueled by rapid developments in faster, denser VLSI application-specific circuits. New processes are creating high-density bipolar chips, VLSI gallium arsenide, fast and very dense CMOS, and, a little further out, BiMOS. Processors optimized for specific tasks—floating-point computation, vector processing, image processing, graphics, database management, information retrieval, simulations of selected models, and running particular programming languages—will be designed to run blindingly fast using these new ASICs.

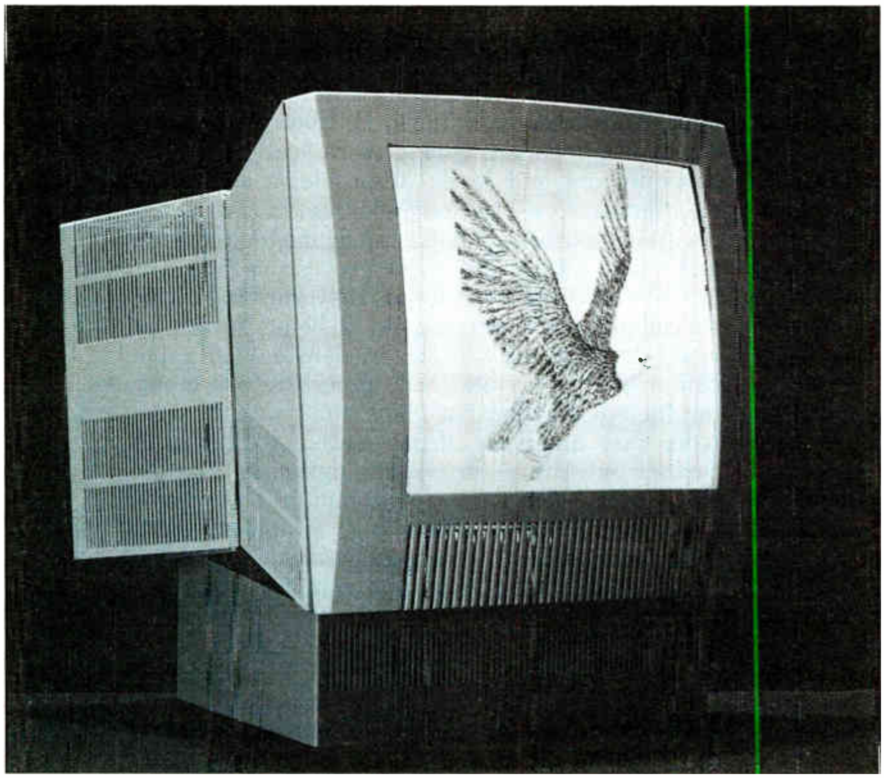
A NEW WORLD OF GRAPHICS

The advent of such power at affordable prices could propel the computer into much more widespread use. In particular, applications that combine modeling, image processing, and realistic color-graphics displays, will increasingly become affordable enough to be used for designing almost anything. They will let designers envision what their product will look like, how it will behave, and how it will stand up without having to make a prototype. They will allow for unlimited tinkering with a design in progress.

This will be a boon to product development in every field. Says Gene Chao, chairman of Metheus Corp. in Hillsboro, "The common theme in



PERSONAL PARALLELISM. More than 40 companies are exploring parallel processing, including Intel, with its Personal Super Computer.



LOTS OF DOTS. Megascan Technology's new monochrome display, at 300 dots/in. (4,096 by 3,278 pixels), offers the highest resolution available in a conventional CRT.

graphics applications is productivity—productivity in computer-aided design, productivity in medical imaging, a thread of productivity wherever graphics is used."

Besides being cheaper, the machines will be easier on their operators, who will have to assimilate the volumes of data that bigger, faster computers generate. A graphics-based user interface speeds things up immeasurably. By graphic manipulation of input information—moving blocks of data, pointing to symbols, manipulating images—a computer user can quickly give instructions. When the computer then presents the result of its action graphically, the operator can quickly react with the next set of graphics-based input instructions.

No matter how big and powerful the departmental computers, special-purpose servers, mainframes, and supercomputers get, though, the computer users of the future will need work stations of many kinds. These will range from personal computers, high-performance PCs, and graphics work stations to a new generation of very high-performance work stations with the power of small supercomputers.

Among the companies developing such new supercomputer work stations are two interesting startups. Dana Computer Corp.—started by Allen H. Michels, founder and former chairman of Convergent Technologies—will give no details of its machine or its timeframe for introduction. But reliable sources indicate that the Sunnyvale, Calif., company is designing its super work station around a RISC-based central processing unit and may use the processor chip set offered by MIPS Computer Systems Inc., also of Sunnyvale.

The other startup is Stellar Computer Corp., also begun by a well-known work-station pioneer: J. William Poduska, a founder of Apollo Computer Inc. Like Dana, the Newton, Mass., company is tight-lipped, but sources indicate that its machine is being built around a proprietary 40,000-gate CMOS gate array.

And three minisupercomputer vendors also introduced work-station versions of the low end of their product lines. They are Alliant Computer Systems Corp., Culler Scientific Systems Corp., and Floating Point Systems Inc.

While super work stations will do more at the desktop, users will still need access to big number crunchers, large data bases, corporate information, or public networks, so these work stations will probably be linked to hierarchical networks of other computers.

SCIENTIFIC COMPUTING

The computers in hierarchical networks increasingly are multimillion-dollar supercomputers, once the rarest birds in computing. Supercomputers and their smaller, more cost-effective cousins, the minisupercomputers, are booming. They are the only machines for which sales are still growing at more than 30% a year. Technically, the trends in these two classes are the same as in other computers: parallel designs, faster, denser ASICs, and other new circuit technologies are spurring this area to new heights.

Cray Research Inc., Minneapolis, the leading light in supercomputers, has three advanced development projects under way to push performance to billions of floating-point operations per second. The first to arrive will be the eight-processor Y-MP, which is expected to deliver 3 gigaflops with up to 500 million 64-bit words of main memory. Priced at nearly $20 million, it may be ready in 1987.

The other projects are a little further out—in time as well as technology. Cray is developing GaAs circuits for the 16-processor Cray-3 program, and industry observers expect a 1988 introduction of a 10-gigaflops machine. The whopper in the wings, though, is a machine called the MP, for which senior vice president Steve Chen is doing a complete new systems design. Estimates indicate that when it is delivered, which could be by 1991, it will run at an astounding 45 gigaflops, using from 32 to 64 processors based on very agressive silicon circuit technology.

Whether it is the world's most powerful supercomputer or the smallest personal computer, a computing machine needs a permanent place to store information. Nonvolatile mass storage devices perform this function. By far the most common today are magnetic disk drives—both hard and flexible. The supporting and bit players in mass storage include magnetic tape drives, videotape recorders, bubble memories, microfilm, and an emerging variety of optical devices.

The optical devices, primarily disk drives of several types, may be the new stars. While the magnetic technologies are well developed, though far from dying, the optical technologies are just beginning to move into commercial production [*Electronics*, May 19, 1986, p. 28].

There are three basic types of optical disk drives: read-only, write-once (non-erasable), and erasable/rewritable. Today, the most commonly used are read-only disks, which come in two formats—12-in. diameter and 4.72-in. diameter. One manufacturer, Reference Technology, makes the 12-in. drives and disks. The 4.72-in. disk—also called a CD-ROM, for compact-disk read-only memory—is made by Hitachi Ltd., Matsushita Electric Co., Denon, Philips International NV, Sony Corp., and Toshiba Corp.

Read-only drives are now used mainly to store and distribute large volumes of information. In the next few years, the major application will probably be as storage for personal computers and work stations. The basic technology of CD-ROMs is unlikely to change—it doesn't need to—but their packaging will be different. Computer systems are now built to work with full-height and half-height 5.25-in. magnetic drives, and future CD-ROM drives will be made in the same format as half-height disk drives. Standard small-computer peripheral interfaces will be incorporated, allowing systems builders to integrate them more easily into small computers.

In displays, flat panels are pacing developments. These units—necessary for portable computers, ideal for certain rugged environments, and desirable in many other applications where their cost/performance ratio makes them feasible—are made primarily from three technologies: liquid crystal, electroluminescence, and gas plasma. Brighter low-power LCDs with wider viewing angles and larger dimensions are on the drawing boards and under test; they will start to show up over the next year. Lower power requirements, lower cost, and bigger EL display panels and some color EL technology are around the corner, too. While these developments take place, the CRT technologies will also improve, especially in terms of resolution. The highest-resolution CRT so far is the recently introduced 300-dot/in. (4,096 by 3,278 pixels) monochrome display offered by Megascan Technology Inc.

Optical disks are going into commercial production, and soon will be packaged in half-height formats, like magnetic disk drives, to work with personal computers

FAST GROWTH OF PARALLEL PROCESSING SURPRISES SEITZ

In the parallel processing field, where a steady stream of new computers and useful applications is emerging, no one is more experienced than Charles L. Seitz. But even he marvels at the pace of parallel processing. "I'm still a little surprised at how quickly it has gone, after years of thinking of it only as experimental." He notes that the technology "crossed the threshold of practicality" during 1985 with so little fanfare that even those persons most deeply involved hardly noticed the significance. "But that's typical of researchers; we're looking at the next problem to be solved" rather than what has already been achieved.

Seitz was a pioneering researcher in the nascent technology in the 1960s, as a graduate student at Massachusetts Institute of Technology. Now a Caltech professor of computer science, he oversaw the design of the experimental Cosmic Cube computer, which emerged in 1983 from a project sponsored by the Defense Advanced Research Projects Agency. It has since evolved into the polished Hypercube architecture, which connects numerous microprocessors that compute simultaneously but independent of the others. The Hypercube is used in parallel-processing machines sold commercially by three companies.

Seitz foresees even more rapid growth because new gear can "piggyback on technology already paid for." The second generation is perhaps two years off, but computing nodes 10 times faster than today's are already in hand.

CHARLES L. SEITZ

Even greater leaps—Seitz won't try to quantify them; the potential for improvement is too great—will come from advances, such as the Torus Routing Chip developed at Caltech, that break the message-passing deadlock of Hypercubes [*Electronics*, Feb. 3, 1986, p. 22]. So, a machine that sends messages virtually as fast as the nodes can process them is close at hand.

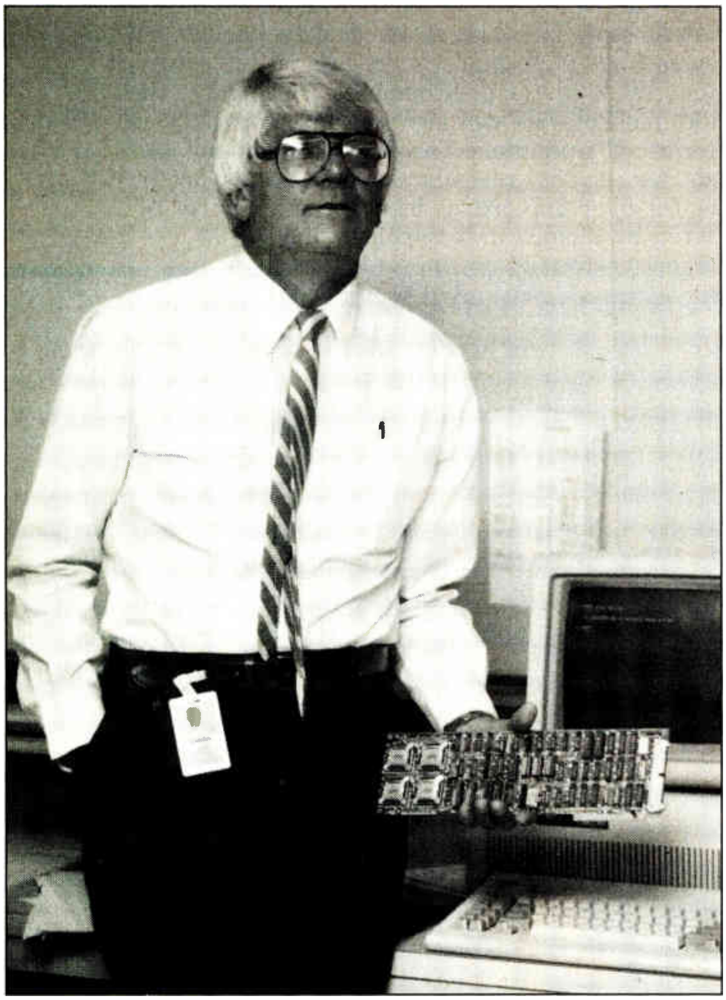
Difficulties in programming parallel processors were supposed to hinder their acceptance. But, Seitz says, "they turned out to be easier to program than most everyone thought," and the machines are already in the hands of programmers, who are churning out software. The next generation of computers will have "boatloads of applications" and the programs to run them.

–Larry Waller

MICROSYSTEMS

The rush is on to develop new systems using the increasingly complex and highly integrated board-level products that are based on 32-bit microprocessors

by Alexander Wolfe



VECTOR BOARD. Zoran president John Ekis holds a powerful processor board built around Zoran's new vector processor.

The big news in microsystems is the on-rush of increasingly complex board-level products that take chips with powerful paper specifications and turn them into working systems. Nowhere is the drive to bring those products to market more intense than in the 32-bit arena, where companies are moving fast to ready their wares. Meanwhile, Intel Corp.'s 32-bit bus standard, Multibus II, is beginning to hit its stride.

Board manufacturers are taking note of the increasingly powerful chips, as well as the higher levels of integration on those chips, to develop a broad range of applications. And digital signal processing is now offering computing power in the 100-ns instruction-cycle range.

For a design engineer, board-level products such as single-board computers offer a powerful lure. He might be able to design a better machine by starting with an individual microprocessor, but ready-made boards obviate the need for expensive and time-consuming hardware design. "You get a finished product and can start developing the software right away," says Gordon Reid, marketing manager at Intel Corp.'s Hillsboro, Ore., Development Systems Operation. The software, says Reid, is what differentiates among machines that are designed around single-board computers.

In the coming year, single-board computers for all the major 32-bit microprocessors should be readily available. Currently, some 20 companies offer boards combining the Motorola 68020 with the company's VMEbus 32-bit bus architecture. Intel Corp. has introduced an 80386 chip on its Multibus II board, and several third-party firms are expected to do the same in 1987.

Other strategies include mixing the chips and buses: Both Heurikon Corp. and Microbar Systems Inc. mate Motorola's 68020 with Intel's Multibus II. No one has yet matched Intel's 80386 with a VMEbus, but that is sure to happen, industry sources say. National Semiconductor's 32-bit microprocessor—the 32332—is also offered on numerous boards.

During the next year, Motorola's VMEbus and Intel's Multibus II 32-bit bus standards will come on strong. It will be a particularly important year for Multibus II, as the first wave of board-level products incorporating the standard becomes available to engineers. "Multibus II is just starting to hit its stride," says Frank Vaughan, a company spokesman.

In technical terms, Multibus II shines. It can transfer data at a top speed of 40 megabytes/s. The transfer rate of the VMEbus is a maximum of 57 megabytes/s, but most VMEbus interfaces run at only 24 megabytes/s, because they transmit data in streams.

"Technically, Multibus II is superior because it's got message-passing ability built into it and it's got an interface which is designed for multiprocessing applications," says Jeff Mattox, senior design engineer at Heurikon Corp. The Madison, Wis., company recently announced its first Multibus II offering, the HK68/M220 board, which allows direct memory accesses at 16 megabytes/s in 16.5-MHz systems, more than twice as fast as many competing boards.

The most significant recent development in microsystems is the increasing integration of functions on boards, a natural result of semiconductor manufacturers packing more and more functions onto a single piece of silicon.

"The functionality that's on one board today used to take five or six boards in the past," says Richard Main, market analyst for Zebu Research Corp., a Sunnyvale, Calif., microsystems market researcher.

But this improvement in microsystems technology has created a paradox for board users. "What [the increased integration] means is that board designers are making choices that the customers used to make regarding what functionality is going to be plugged together. The result is these things are less flexible, less of a perfect fit than they were in the past. Customers don't like that, so they're being very specific about their needs," says Main. As a result, a large number of board companies have sprung up to meet specific customer needs in specific niches—for example, board-based controllers for local-area networking.

The technology of digital signal processing is also developing rapidly. DSP chips, like microprocessors, offer ample computing power. But their architecture and instruction sets have been optimized for solving problems that rely on digital filtering techniques as well as heavy number crunching. Typical applications for DSP chips and boards include telecommunications, numerical processing, spectral analysis, two- and three-dimensional imaging, and speech recognition and synthesis.

During the past year, an array of powerful DSP chips was introduced. Motorola's highly parallel CMOS chip, designated the DSP5600, can execute 10.25 million instructions/s at clock rates of 20.5 MHz. Analog Devices Inc. introduced the ADSP-2100 programmable DSP, which features 1.5-μm CMOS technology containing a 16-by-16-bit multiplier, a 40-bit accumulator, a program sequencer, two data address generators, and an arithmetic logic unit; it boasts a 125-ns cycle time.

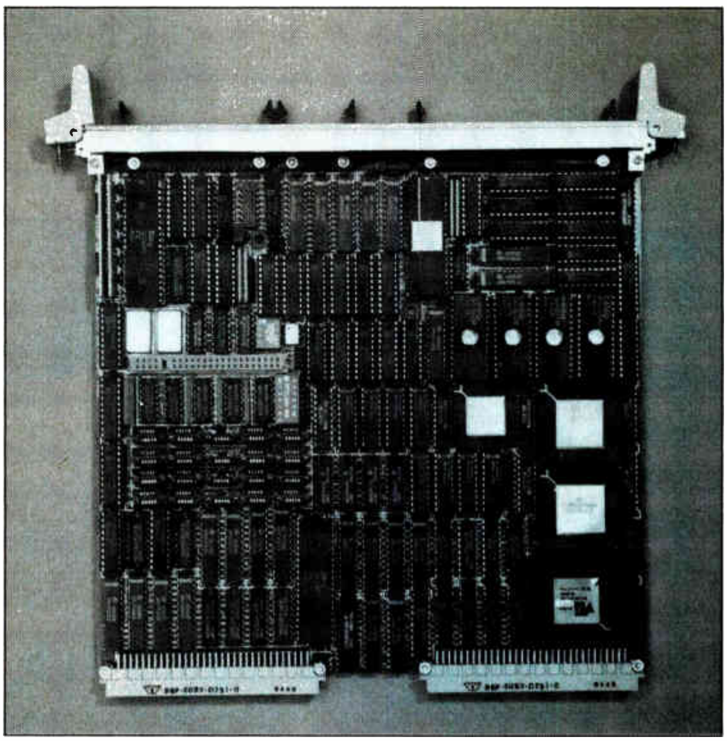
Texas Instruments unveiled its fastest DSP yet, the TMS320C25, which features a 100-ns cycle time. National Semiconductor Corp. announced its own 100-ns DSP, the LM32900, which also features a software-assisted floating-point multiplier.

Philips International NV, Europe's leading integrated-circuit maker, brought out the first two members of its SP50 family of DSP chips. Both chips feature a pipelined Harvard architecture and an instruction cycle time of 125 ns. And

Because of the levels of integration that chip makers are reaching, the functionality that used to require five or six boards can fit on one board today

Zoran Corp.'s ZR34161 uses vector-handling techniques to boost speed, while embedded signal-processing algorithms cut system overhead—allowing the ZR34161 to calculate a fast Fourier transform in only 2.5 ms [*Electronics*, July 24, 1986, p. 59].

Many of these new, supercharged DSP chips will find their way onto boards during the coming year. Such boards will undoubtedly become the heart of powerful, dedicated signal-processing computers aimed at solving problems in speech synthesis, speech recognition, and artificial intelligence.

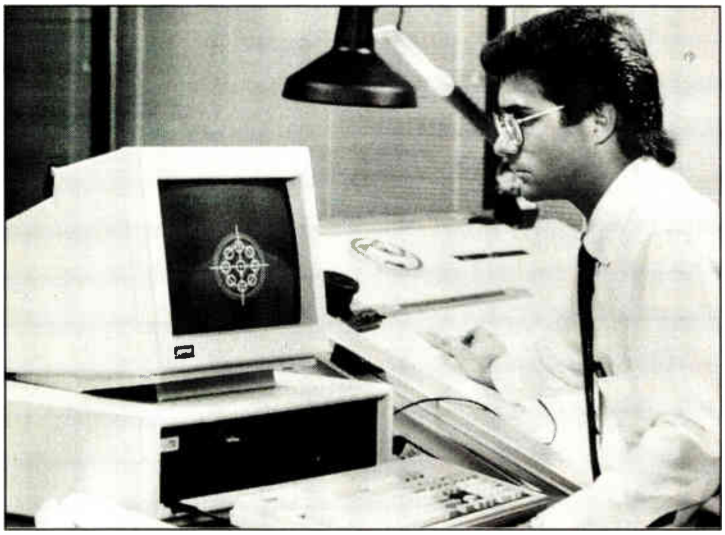


BUS BOARD. Heurikon Corp.'s first Multibus II offering, the HK68/M220 board, allows direct memory accesses at 16 megabytes/s in 16.5-MHz systems.

SOFTWARE

Software engineers will face the challenge of writing programs that harness the potential of artificial intelligence and the power of a new generation of hardware

by Alexander Wolfe



HAND IN HAND. The appearance of ever-more-powerful computers has enabled software engineers to turn out increasingly sophisticated programs.

Driven by the power of hardware and the potential of artificial intelligence, software engineers are breaking new ground. With hardware more muscular than ever, software engineers now have at their fingertips the horsepower needed to turn out ever more sophisticated programs. At the same time, they have a very pragmatic task: to develop programs that fully utilize this hardware, lest the new machines sit all revved up with nothing to calculate.

A major source of software excitement is AI. Over the past year, designers have increasingly looked to this technology as the next wave, despite the continuing debate over whether expert systems have lived up to the lofty expectations voiced by many people a year or two ago [*Electronics*, Aug. 7, 1986, p. 59].

The microcomputer retains its luster, especially with the recent introduction of Intel Corp.'s 32-bit microprocessor, the 80386. This market anxiously awaits a major new release in early 1987 from Microsoft Corp., as competitors nip at that company's heels in the rush to create operating-system software for the new 32-bit machines.

Another area spurring software innovations is AT&T's venerable Unix operating system. Unix continues to gain users and is expanding into networking. Designers are likewise turning their attention to the increasingly sophisticated real-time executives and kernels, which manage fast-response computer systems.

Leading off the new software season is a big vote of confidence for AI from none other than IBM Corp. After years of sitting on the sidelines, IBM has finally jumped into AI software in a big way in the form of a massive joint research project with Carnegie Mellon University in Pittsburgh [*Electronics*, Aug. 21, 1986, p. 21].

Herbert Schorr, group director for products and technology for IBM Corp.'s Information Systems and Storage Group, believes that AI holds the key to the next generation of software. "Knowledge[-based] systems are the second wave of data processing," he says. A branch of AI, knowledge-based systems incorporate information gleaned from human experts directly into software. This software can then make decisions about how to perform complex tasks, often those

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FOR SCHORR. IBM's Herbert Schorr believes AI is the key to the next generation of software.

that fall into the gray or "fuzzy" region where there are no simple yes or no answers.

"We've [already] taken the back-office tasks and started to computerize them," says Schorr. But with few exceptions, he says—such as airline reservations systems—"we haven't [computerized] the front-end or 'mission-critical' tasks." The missing link will be supplied by knowledge-based systems. When added to database and communications facilities, they will make possible the computerization of the front end of the office, Schorr believes. This task will be aided by the wide range of expert-systems development tools currently on the market.

The personal computer will lose none of its importance in the coming year. Microcomputer software continues to mature, and so do the companies that make it. One sign of that maturing is the recent decision by two California companies—Ashton-Tate and Software Publishing Corp.—to remove copy protection from their products. The intention is to win friends among

One of the most eagerly awaited software events of next year is the introduction of MS-DOS 5.0, which is supposed to support Intel's new 32-bit 80386 microprocessor

corporate users, who have made it clear they don't like wrestling with the cumbersome access keys needed to use protected software.

Perhaps the most eagerly awaited microcomputer software event of 1987 is the release of MS-DOS 5.0 from Microsoft Corp. The Redmond, Wash., software house is said to be readying the next version of this standard operating system for the IBM Personal Computer and compatibles.

MS-DOS 5.0 is reportedly designed to support Intel's 80286 microprocessor, but it will also support the 80386, the powerful new 32-bit microprocessor, basically by treating it as a fast 80286. The 80386 is at the heart of Compaq Computer Corp.'s new Deskpro 386 computer, and is sure to crop up in more computers and work stations over the next year—20 to 30 machines based on it are expected to be introduced [*Electronics*, Sept. 18, 1986, p. 91].

Also pushing software engineers toward new designs is AT&T's Unix System V release 3.0. The latest version of the operating system has a number of new features that add power to networking applications. Thousands of developers and users will be examining these new twists when they convene for the three-day Unix Expo in New York next week.

Much of the discussion there will center on the Streams I/O facility and Remote File Sharing. Streams, which frees applications software from any dependence on hardware, enables character input/output to be implemented in a modular way, with well-defined interfaces to the Unix kernel architecture. By writing separate modules for different network configurations, programmers can incorporate modules that implement particular communications standards (for example, Ethernet) into their software packages, without having to modify their applications programs. Remote File Sharing allows transparent file sharing across a network; a user can access files and data on remote computers as if they were on the local machine.

Unix will get an additional boost from efforts to standardize the interface between the operating system and application software. An IEEE committee is currently at work on that task. Such standardization will make it easier for C programmers to develop portable applications software that can run on any Unix machine without modification.

Integration is another trend to watch. "The integration of MS-DOS, Unix, and local- area networks to solve departmental computing problems is coming to fruition," says Bruce Weiner, president of /usr/ group, Santa Clara, Calif. "There are now network products available that, from a PC running MS-DOS, let you access full Unix systems as if you were connected straight to them."

A host of smaller operating systems—the real-time executives and kernels—are also on the move. In this market, the challenge is to upgrade systems to tackle tougher tasks, and a number of companies are working toward that aim. They include most of the major computer makers—including Data General Corp., Digital Equipment Corp., and Harris Corp.—as well as such software firms as Forth, Hunter & Ready, Industrial Programming, JMI Software Consultants, and Whitesmiths.

"Industry-wide, there is an emphasis on the high end of things," says Bernard Mushinsky, president of Industrial Programming, Jericho, N. Y. "The problem of the small application has already been solved, and there are numerous choices in [operating systems]. But high-end applications—involving imaging systems, signal processing, and multiprocessors—really need other solutions, and I think that there will be more emphasis on that and more far-reaching developments that will help people do those things," he says.

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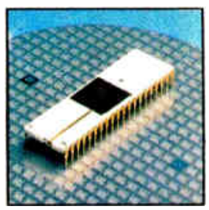

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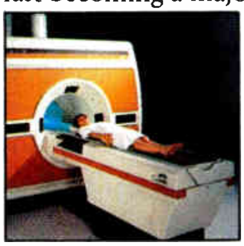

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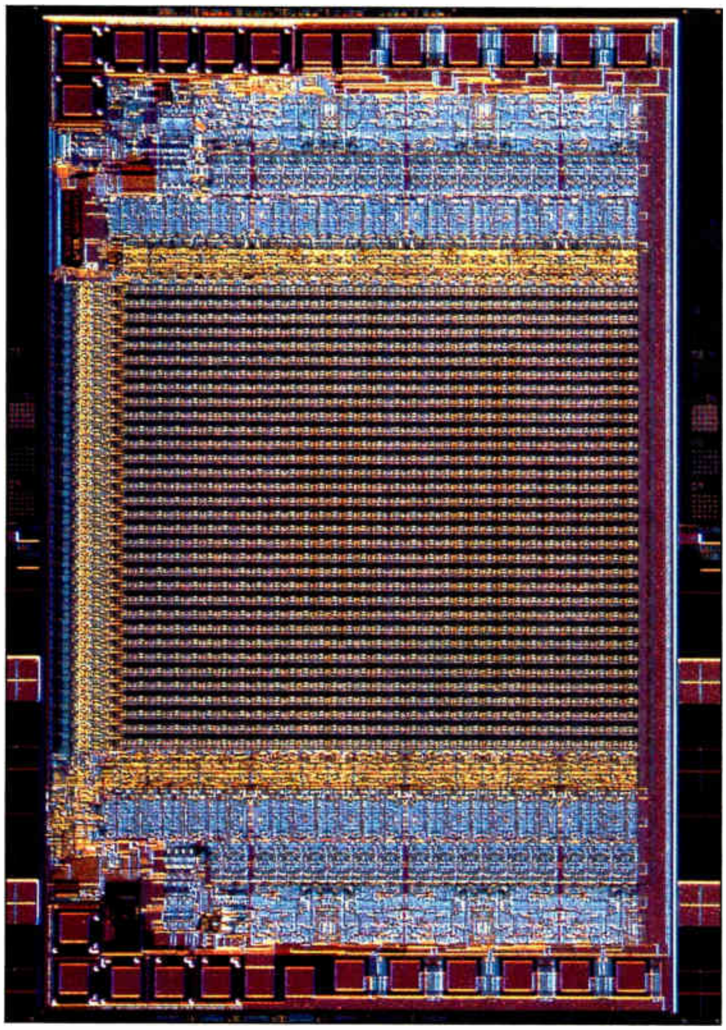
SEMICONDUCTORS

Memories continue to surprise, while semicustom ICs are changing dramatically; in processes, gallium arsenide will strengthen as a contender with silicon

by Bernard Conrad Cole



ERASABLE ASIC. By eliminating AND/OR gates in its 78C800 IC, Excel in effect creates erasable application-specific ICs—Erasics.

The semiconductor industry can always be counted on to surprise, and the coming year will be no exception. Marketplace competition should be fierce, especially in DRAMS and SRAMS. At the same time, manufacturers are pushing technology to the limits and experimenting with new solutions in an attempt to improve both standard parts and custom and semicustom integrated circuits.

Illustrative of the anticipated ups and downs is the tumult in the memory marketplace, where the 256-K dynamic random-access memory is beginning to lose ground to the 1-Mb DRAM.

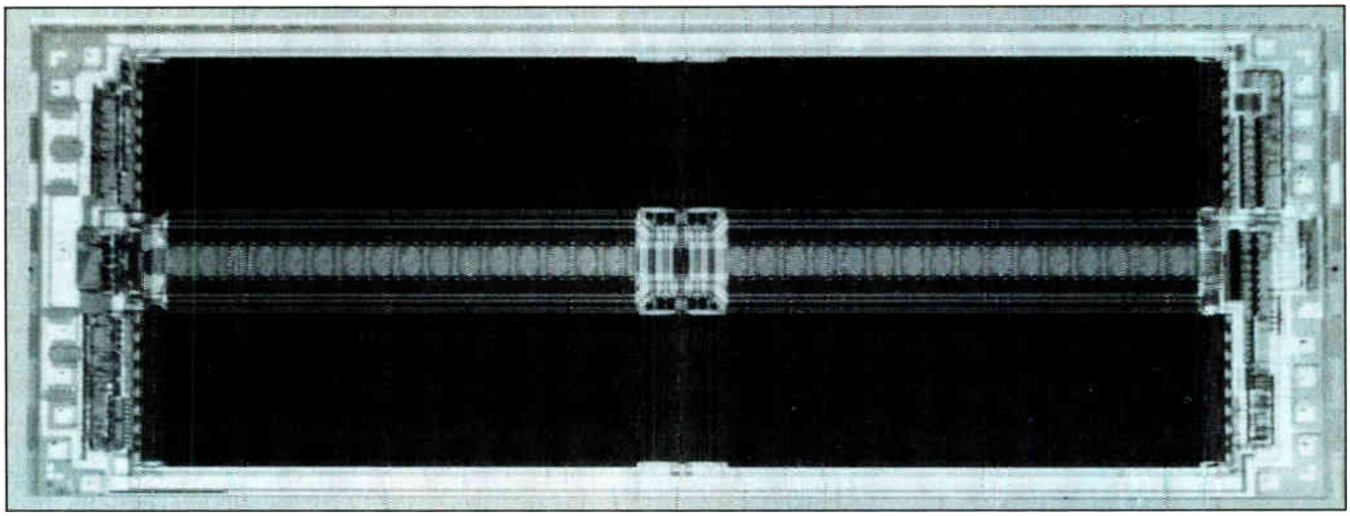
The 1-Mb devices weren't expected to enter the marketplace in volume until at least 1988, and at the beginning of the year only a half-dozen varieties were being sampled by three or four vendors. By the first quarter of 1987, though, almost a dozen suppliers will be producing volume quantities of more than 50 such devices.

"If you thought the price attrition in 64-K and 256-K DRAMs was bloody, wait until you see what happens in 1-Mb DRAMs," says Andrew Prophet, semiconductor industry analyst at Dataquest Inc., San Jose. "Fortunately, most of the competition will be between Japanese and Korean companies." But such U. S. manufacturers as AT&T, Micron, Texas Instruments, and Vitelic will also be market participants.

For both economic and technical reasons, the move to 4-Mb designs will be somewhat slower, says Sarge Grewall, MOS memory marketing manager at National Semiconductor Corp., Santa Clara, Calif. "Considering the multimillion dollar expense of setting up production facilities for each succeeding generation," he says, "there is not an awful lot of incentive for a company to make the investment if all that can be expected is pricing that is cut to the bone."

A FIGHT FOR DOMINATION

Things are heating up in DRAMs, but competition will be fiercer in static RAMs, where process technology is being pushed to its limits. By the end of the year, at least two 1.25- to 1.5-μm 256-K CMOS SRAMs will be available in sample quantities, and two more will be available in sample quantities by the end of the first quarter of 1987. The earliest introductions, both with access times approaching 50 ns, are from Advanced Mi-



FIERCE COMPETITION. As 1-Mbit DRAMs like this one from TI reach the market in volume, competition will drive down prices.

cro Devices Inc. and Lattice Semiconductor Corp. In low-density SRAMs—1-K, 4-K, and 16-K—submicron CMOS is battling it out with gallium arsenide, silicon bipolar, and mixed BiMOS designs.

Today, silicon bipolar emitter-coupled logic is the dominant factor in high-speed SRAMs—1-K and 4-K memories with 5- to 10-ns access times. Now emerging from research and development are 1-ns to 5-ns designs in memory sizes ranging from 1-K to 16-K, says Madhu Vora, director of bipolar research at Fairchild Semiconductor Corp., Palo Alto, Calif.

Working to keep pace are companies such as Cypress Semiconductor Corp., where president T. J. Rodgers reports that state-of-the-art 1.25- to 1.50-μm CMOS technology is yielding high-performance chips. Rodgers says the San Jose company has production quantities of 10-ns to 15-ns 1-K and 4-K TTL-compatible SRAMs. Further scaling to 1 μm and below, he says, will yield 4-K designs with access times below 10 ns and 1-K designs below 5 ns.

A new factor in the SRAM market during the coming year will be gallium arsenide, says Lou Tomasetta, president of the Semiconductor Division of Vitesse Electronics Corp., Camarillo, Calif. Scheduled for production in at least sample quantities are 1-K and 4-K GaAs SRAMs in the 1.5-to-3.0-ns range, he says.

Bridging the cost/performance/power gap between GaAs and bipolar silicon SRAMS will be a wide variety of mixed-process BiMOS parts from companies such as Hitachi and NEC, says Ray Hawkins, vice president of marketing at Saratoga Semiconductor Corp., Cupertino, Calif. Also participating will be a number of American firms, including Saratoga, Fairchild Semiconductor, Texas Instruments, and Motorola.

Adding further to the tumult in the memory marketplace, says Dataquest's Prophet, will be the emergence of a wide variety of application-specific SRAMs and DRAMs into production. The new offerings will include RAMs with mask-programmable architectures, multiport RAMs, intelligent memories, dual-array memories, content-addressable memories, RAM-based cell arrays, and mixed gate-array and RAM combinations in a variety of architectural configurations.

Gains in both density and speed will continue next year in UV and electrically erasable PROMs, featuring near 1-μm geometries and programming cells that are one-fourth the size of current devices—down from about 200 μm^2 to less than 50 μm^2.

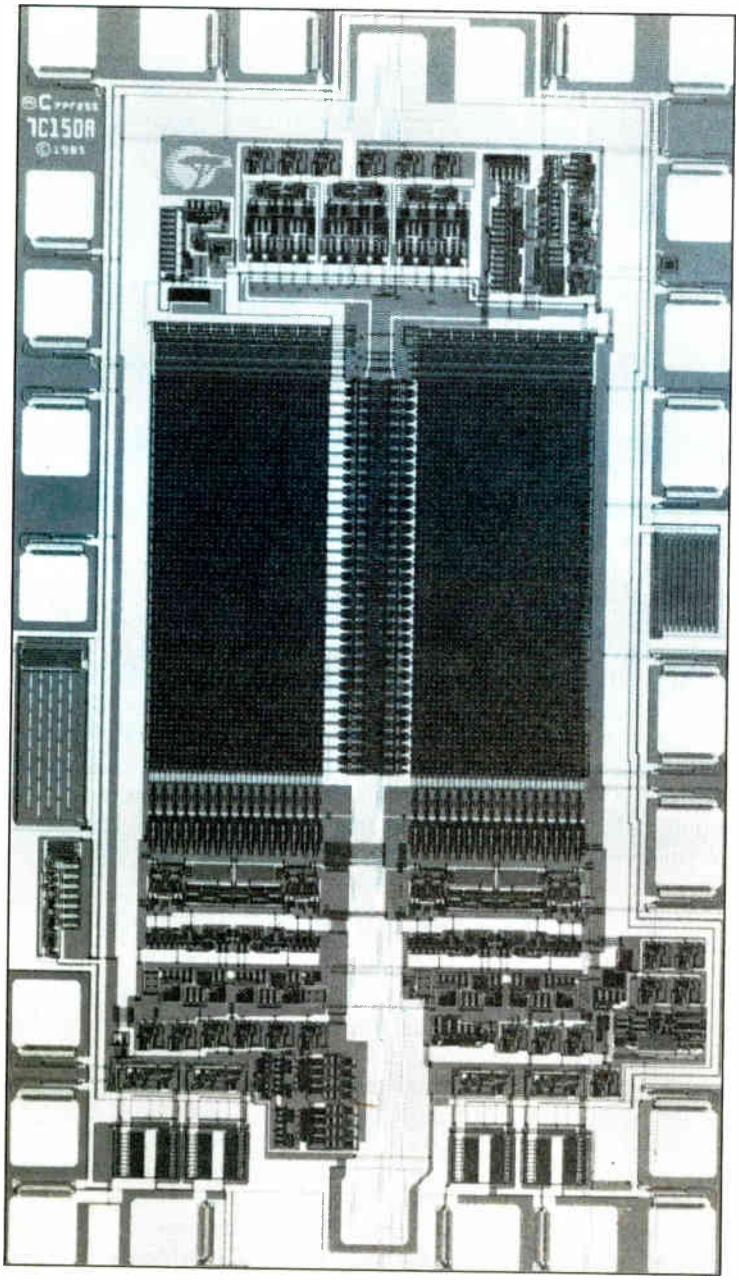
With such improvements, EEPROMs in particular offer the possibility of challenging SRAMs in some applications, says Richard Pashley, general manager of Intel Corp.'s EEPROM technology development in Folsom, Calif. "Although EEPROMs are not ideal for all applications, they offer distinct advantages to other memories," he says. "They hold the edge over byte-wide statics in that they are an all-silicon solution to nonvolatility, whereas SRAMs need a battery to operate."

More important, he says, EEPROMs will soon be able to capitalize on the fact that their memory cells are smaller than those of SRAMs, which use four to six transistors, compared to EEPROMs, with the equivalent to 1.5 to 2 transistors. As a result, EEPROMs will soon surpass SRAMs in density, improving their cost-effectiveness, he says.

ASICs, EPLDs, AND ERASICs

In semicustom circuits, a major effort will be made during the next year to develop techniques for increasing the number of usable gates while also speeding turnaround time from design to fabrication. This will be particularly important for gate-array vendors, who are beginning to feel the heat from the inherently denser standard-cell methodology.

The key to the standard cells' denser circuits is that all layers can be customized, explains Alex Young, vice president of engineering at Zymos Corp., Santa Clara. In gate arrays, only



FAST ACCESS. The Cypress Semiconductor 1-K and 4-K CMOS SRAMS have access times from 10 to 15 ns.

the last one or two mask steps can be customized. This results in varying gate utilization—in standard cells, it's virtually 100% for densities up to 50,000 gates; for gate arrays, the utilization rate wanders from a low of 25% to 30% at densities of 50,000 or more, up to 60% to 75% at densities of 15,000 and below.

Because interconnection channels can take up as much as 50% to 65% of a chip's area, gate-array companies are seeking to eliminate such channels by running lines over or through the active gates. Variously called butted gates, sea-of-gates, channelless arrays, or compacted arrays, this approach can double gate utilization. Dan Yoder, ASIC product manager at VLSI Technology Inc., says the result is a virtual 100% utilization at low densities. Above 25,000 gates, though, utilization is still no more than 50% to 60%. "As a result, much effort will be expended during the next year to improve this utilization rate without sacrificing the gate array's turnaround advantage over standard cells," he says. Two methods are improving the automated placement-and-routing software, and improving the basic array architecture.

Another digital product area in for some dramatic changes is field-programmable logic. The industry is moving away from bipolar-based fusible-link PLDs and toward CMOS-based PLDs, using either ultraviolet or electrical erasure mechanisms. Concurrently, synergistic combinations of gate arrays and standard cells are being developed. Currently, EPLDs from companies such as Altera Corp. and Lattice use the fixed-OR, programmable-AND array structure invented by Monolithic Memories Inc. in its bipolar fusible-link PAL programmable array logic. Using 1.5- to 2.0-μm CMOS, Altera, Intel Corp., and others have achieved gate densities of up to 2,000 or so in UV-based EPLDs. Lattice and others have achieved up to 1,000 gates in electrically erasable versions.

A LOT OF SOFTWARE

The chief advantage of such AND/OR-based EPLDs is that there is a multitude of software development tools available, says George Landers, director of marketing at Exel Microelectronics Inc., San Jose. "However, AND/OR-type gates are best suited to bipolar technology," he says. "When transferred to CMOS, it actually costs you in terms of density, functionality, and flexibility." This is because the natural building block for CMOS is the NOR function; to build AND/OR-type EPLDs requires adding circuitry to invert the input polarities. "Eliminating this additional level of complexity increases the gate density beyond what is available with current CMOS AND/OR EPLDs, approaching the gate-array densities—creating, in effect, erasable ASICs, or Erasics," he says. Similar efforts are under way at Signetics Corp. and Monolithic Memories Inc.

As both bipolar and MOS technologies move toward the submicron region, chip designers will be faced with a ticklish decision. According to Sunlin Chou, director of technology development at Intel Corp. in Aloha, Ore., they will have to decide whether or not to abandon the current 5-V operating voltage that has become standard in the industry. If the 5-V standard is retained, manufacturers are faced with developing much more complex and expensive processes to avoid such fundamental device physics constraints as punch-through, gate dielectric breakdown, and hot-electron effects. But if voltages are scaled down along with chip geometries, many of these problems disappear.

The major issue in scaling voltages is compatibility with current TTL-interface standards, Chou says. "Previous reductions in operating voltage, from 18 to 12 to 10 to the present 5 V, only made LSI and VLSI circuits more compatible with the 5-V TTL standard. Further reductions move the technology away from that standard." But Chou believes the advantages outweigh the difficulties. "While some aspects of circuit design are made more difficult by scaling voltages," he says, "these are outweighed by improved density, simplified processing, and enhanced power/-performance ratios."

In general, Chou says, designers agree that the next power-supply standard should be set at about 3.3 V, enabling devices to interface directly with TTL-level components in a system. Much lower than that, he says, such compatibility is not possible. But there is disagreement on how to implement submicron VLSI digital circuits.

GaAs OR SILICON?

Although gallium arsenide is beginning to emerge as a viable VLSI technology, some questions still remain as to its mainstream potential, mostly because of its higher cost [*Electronics*, Sept. 18, 1986, p. 57]. Also, the technology is more complex, and materials scientists and electrical engineers have yet to master the more complicated GaAs processes to make high-quality, low-cost material that is competitive with silicon.

In the works, however, are technological developments that may change this equation. Particularly important is the increasing commercial viability of growing epitaxial crystalline GaAs layers on silicon substrates to combine the best of both worlds, says Bob Gisburne, GaAs custom products manager at Ford Microelectronics, Colorado Springs, Colo.

Researchers in the U. S. and Japan can now make GaAs-on-silicon wafers that come close to matching the quality of conventional GaAs. In exchange for the extra complexity, manufacturers will gain a number of advantages, including the better mechanical and thermal properties of silicon compared with GaAs.

Because silicon is less brittle, combination wafers are less fragile and easier to handle than wafers of pure GaAs, resulting in lower-cost dies. Taking advantage of the higher thermal conductivity of the underlying silicon to allow more uniform removal of heat from solidifying crystals, it should soon be possible to grow GaAs/Si wafers two to three times the current 3-in. diameter of GaAs, noticeably lowering costs. The higher thermal conductivity also means quicker dissipation of heat generated by the transistors, which allows more devices to be integrated onto a GaAs chip—increasing the density and lowering the cost per bit and per gate.

GaAs-on-silicon wafers could combine the best of both worlds: the much higher speed of gallium arsenide and the better mechanical and thermal properties of silicon

PROUD PAPA CAVLAN WATCHES PROGRAMMABLE LOGIC GROW UP

Napoleone Cavlan became became known as the father of programmable logic arrays—a type of field-programmable logic device—during his 10 years with Signetics Corp., where the first successful ones were developed in the mid-1970s.

Cavlan, 47, jokes that he got the title by pacing corridors like any expectant father. To popularize the technology when he was the Sunnyvale, Calif., company's PLA applications manager, Cavlan talked to systems designers in countless conference halls and electronics plants. But he also invented integrated fuse logic and helped conceive such PLA variations as register-paced logic sequencers for tailored controllers, and he was product-architecture manager while Signetics led the trend to high-density programmable macrologic.

However, his PLA was overtaken in the marketplace by John Birkner's PAL, or programmable array logic, a simplified array invented at Monolithic Memories Inc. of Santa Clara, Calif., by Birkner and H.T. Chua. At first, says Cavlan, he and Birkner were adversaries on the conference circuit, "but we came to realize that we shared a common vision and developed a cordial professional relationship." Birkner (who left Monolithic Memories this year to become a consultant) urged him to join Monolithic Memories, and last February, Cavlan became its manager of PAL product planning. He made the move, he adds, because Monolithic Memories is not only the market leader but also is "more adventurous."

NAPOLEONE CAVLAN

Cavlan is convinced that manufacturers combining structured logic and programmable arrays are on the right track. Monolithic Memories will soon join them with programmable sequencers. It has also obtained a license to employ a CMOS reconfigurable logic concept developed by Xilinx Corp. of San Jose, Calif.

To carry the structured approach a step further than the state of the art, Cavlan is exploring new ways of integrating large logic elements with small programmable arrays. Conceptually, the devices would be islands of higher-level logic in a tailorable stream of signal paths and random-logic glue. In this way, he believes, functional density can be multiplied without complicating system design tasks. *–George Sideris*

CHIP PROCESSING

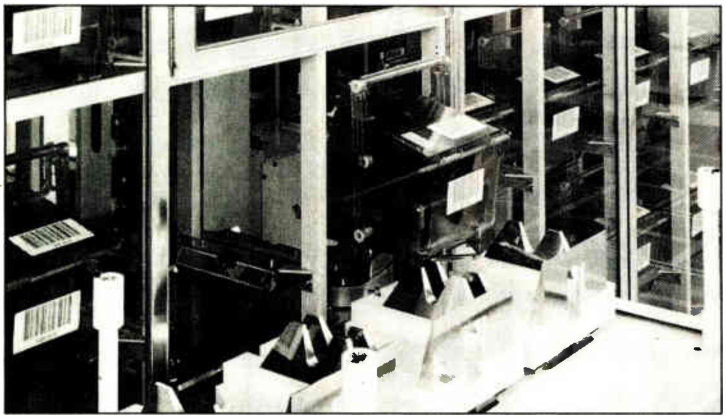
The push to create an ultra-clean environment and the search for commercial X-ray lithography will dominate semiconductor processing

by Jerry Lyman

In the field of semiconductor processing, two developments stand out as the key areas to watch in the coming year: a major effort to create super-clean environments and noncontaminating machines; and a concerted drive to develop commercial X-ray lithography.

The movement toward super-cleanliness comes in part from the Defense Department's Very High Speed Integrated Circuits program. Part of the commercial fallout of Phase 1 of VHSIC is that companies such as Honeywell's Solid State Division, Martin Marietta, Texas Instruments, TRW, and others put together advanced 1.25-μm IC fab lines with Class 10 clean rooms, which are absolutely necessary to get any sort of yield on the near-micron chips.

Until recently, these IC lines were among the cleanest in the U. S. Now TI has built two even cleaner facilities, identical fabs in Dallas and Miho, Japan, at a cost of more than $100 million each. Designed to fabricate advanced MOS memory devices, they boast super Class 5 clean rooms (no more than 5 particles/cubic foot larger than 0.2 μm).



CLASS 5. At TI's Class 5 semiconductor processing facility in Dallas, automated guided vehicles reduce human contact with the processed silicon wafers.

TI's original aim was to meet the vibration requirements compatible with the Class 5 specifications and to reduce the particle count in the processing areas by automating wherever possible. In fact, the company surpassed its goals, creating the equivalent of a Class 1 clean room.

Semiconductor equipment makers are also attacking the particulate problem. For example, both Applied Materials Inc. and Perkin-Elmer Corp. offer equipment with guaranteed particulate counts.

Applied Materials guarantees that its 8300 aluminum etcher will generate fewer than 0.1 particles/cm^2 per wafer pass. Perkin-Elmer has designed its Micralign 600 HT stepper so that for a 125-mm wafer, this aligner is specified at 15 particles per path.

X-RAY LITHOGRAPHY ADVANCES

In the other important development of the year, X-ray lithography is gathering steam on many fronts. In the U. S., Micronix Corp. has developed the MX-1600, the first commercial X-ray stepper. Perkin-Elmer is supplying the same type of machine to the VHSIC program [*Electronics*, March 17, 1986, p. 46]. Both units are based on conventional X-ray sources, but in the next few years the technology will probably go to higher-power plasma X-ray sources. More advanced work is being done by a team from IBM Corp., which is investigating synchronous technology using the National Synchrotron Light Source at Brookhaven National Laboratory.

But the world leader in synchronous X-ray lithography is West Germany. Under the direction of the Fraunhofer Institute for Microstructures Technology, West Berlin, and a consortium of semiconductor makers, West Germany has mounted an ambitious program that has just gone commercial. The company created by this effort, COSY Microtec GmbH in West Berlin, expects to deliver by 1988 a compact storage ring suitable for X-ray lithography.

Striving to catch up, Japan has initiated a 13-company cooperative effort called Sortec, which will build a synchrotron center for X-ray lithography research by its members.

TELECOMMUNICATIONS

Field testing and component development will accelerate for the all-digital phone network, and voice-recognition systems will make slow but steady progress

by Robert Rosenberg

In the world of telecommunications next year, the prime technological mover will be the integrated services digital network—the plan to replace the world's analog telephone network with an all-digital net. Important field trials in the U. S will test new ISDN equipment and services and prove out the silicon support coming from U. S chip makers.

On other fronts, researchers are making big strides in speech recognition. And the forward thrust of satellite communications has not screeched to a halt, despite the explosion that destroyed the space shuttle Challenger.

Most of the ISDN action next year is expected to continue to focus on development of chips for the customer-premises—the S/T interface. Among the 10 or so silicon makers that have announced or are shipping silicon to support ISDN, almost all have limited their offerings to the customer-premise or PBX markets. The focus of these chip makers is not likely to change next year, since there is no agreement on a standard for the U interface between the central office and the local loop to a subscriber's equipment. The difficulty of reaching a consensus and establishing a standard for the U interface stems from the fact that all the interested countries have different designs for their local loops. Any international standard must work across all these loops, a knotty political problem for the International Telegraph and Telephone Consultative Committee.

For chip makers already committed to the ISDN, the challenge in the year ahead will be to drive down the cost per connection while continuing up the curve toward greater levels of integration. The biggest hurdle is the line frame, the portion of the PBX where the codecs and line cards are located. It accounts for 50% of the average cost of the components in a PBX switch.

Meeting the challenge, for example, is Advanced Micro Devices Inc. It is already applying its 1.6-μm CMOS process to the Am79C31 digital exchange controller for the line

TALKING TYPEWRITERS. Large-vocabulary voice recognizers, like the prototype shown by IBM, may hit the market as early as next year.

frame, as well as to the Am79C30 digital subscriber controller for customer equipment. In 1987, AMD plans to bring features below the 1-μm level, driving down costs, says Ron Ruebusch, director of strategic marketing for communications products.

Over the next year, the current crop of ISDN circuits are likely to evolve, as will the designs of the gear first used in the field trials. For example, makers of telecommunications equipment developing products for the early ISDN field trials are finding they have few options when it comes to interface circuits, says Al Mouton, Motorola Inc.'s MOS telecommunications manager. That means switch houses are relying on prototype chips, knowing a different ISDN chip set might be used in production equipment.

Speech-recognition systems that handle limited vocabularies are moving into industrial settings, and R&D attention is focusing on large-vocabulary systems

Some of these early prototypes will show up during next year's field trials scheduled by Mountain Bell in the greater Phoenix area. These field trials will provide a showcase for the major makers of central office switches and will also show off much new telecom gear using the new ISDN circuitry. For example, Northern Telecom will be testing its DMS-100 central-office switch connected by 200 2B+D channels to a variety of work stations and terminals provided by various manufacturers.

The field trails also should provide the first peek at the new generation of ISDN integrated voice-data terminals. Customers with new integrated voice and data terminals can receive voice calls on the B channel with full internetworking to non-ISDN voice channels. Circuit-switched data connections on the B channel will have a full 64-Kb/s clear channel to other ISDN links. The 16-Kb/s D channel will support signalling and packet switching.

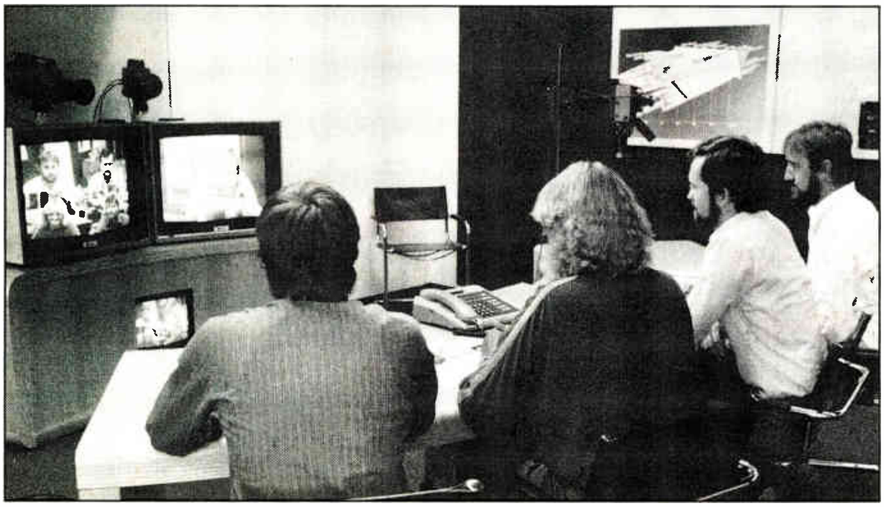
Another important Mountain Bell test scheduled for early next year in Phoenix will be a trial of fiber optics in a local loop. The broadband characteristics of fiber could push ISDN into consumer applications such as high-definition TV. The same characteristics could make fiber optics more useful for business customers with heavy data requirements, such as a distributed computer-aided-design network.

"The trunk lines and the long-haul sections [of a nationwide optical net] are nearing completion," says J. E. (Jack) Andrews, department chief of Lightguide Division Engineering, AT&T Network Systems, Norcross, Ga. "Now we are going into the distribution-system phase [of deployment] such as fiber in the local loop."

As part of the test of fiber in the local loop, Mountain Bell plans to link an AT&T No. 5 ESS digital switch to a remote optical module for the Phoenix field trial. This will help establish whether customer-premise broadband connections and remote electronics that perform video encoding and decoding and optical-signal transmission can become more widely deployed. Though the second generation of ISDN probably won't be deployed till the 1990s, the Phoenix test of broadband fiber is expected to provide important data about how quickly B-ISDN, or broadband ISDN, can come about.

Another area of communications technology that will rack up solid advances is speech recognition—endowing machines with the ability to interpret and act on human speech. Small-vocabulary systems, which process a limited vocabulary of distinctly uttered words, have already begun to move into industrial settings. But the biggest plum in recognition—large-vocabulary systems—is still waiting to be picked. They could turn voice recognition into a billion-dollar industry by the end of the decade. Working as a front end to, say, a word processor, large-vocabulary systems may one day replace the keyboard. Several companies, including IBM Corp. and Dragon Systems Inc., are developing systems now. At least one could hit the market by next year.

IBM Corp. has been pouring money into voice-recognition research for years. This year, the Armonk, N.Y., company began shipping its voice-communications option for the IBM Personal Computer. With a printed-circuit card and the right software package, users can speak PC-DOS commands or digitize an incoming call, store it, then call up a listing of all the calls on screen and



FUTURE ISDN. Full motation video conferencing using broadband in the local loop could come as early as the 1990s.

select one for playback. Though its abilities are limited, the underlying speech-recognition algorithms—which are based upon a predictive model of how English is spoken—hold much promise.

The heart of the PC voice-recognition option is the stochastic model of speech developed by Dragon Systems. Stochastic modeling is a statistical tool that models the probabilistic nature of various phenomena. When applied to language processing, it looks at the contextual nature of acoustical and language information in speech. It characterizes the probability of certainty of that information and quantifies it. The quantified information is compared against information the system has previously gathered as it analyzed the spoken words; it then makes a decision as to what it has just heard.

A 10,000-WORD GOAL

Dragon itself is producing recognition systems, and it has begun shipping a discrete-word recognizer with a 1,000-word vocabulary. The Newton, Mass., company is continuing to refine its recognition algorithm code and expects to have software able to handle a vocabulary of 10,000 to 20,000 words, possibly as early as next year, says president Janet Baker. Dragon is also working on a 10,000-word algorithm in silicon for the Defense Advanced Research Projects Agency, but little detail is expected to emerge in the next year on this classified project.

IBM has also made some notable voice-recognition advances on its own. Two years ago, the company's speech-processing group used an IBM 4341 computer and three Floating Point Systems 190L array processors to recognize a 5,000-word speaker-dependent vocabulary. Now seven speech-processing boards built with off-the-shelf digital signal processing ICs in a Personal Computer AT do the job.

"We will build several more boards this year, then begin a series of human-factor tests that will last till the end of next year," says Fredrick Jelinek, speech-processing team leader at the Thomas J. Watson Research Center in Yorktown Heights, N. Y. It is likely that work on custom silicon is already under way at IBM, and that the seven boards will be reduced to a handful of chips before a final product emerges.

In communications satellites, the pace of technological innovation has not slowed, despite drastic delays in launches in the wake of the Challenger disaster, the explosion of a Titan 34D in April, and the crash of a Delta rocket in May. All three spacecraft are prime vehicles for the launch of satellites.

For example, Ford Aerospace & Communications Corp.'s operation in Sunnyvale, Calif., is pushing ahead with plans for commercial satellites now on the drawing board, and Hughes Aircraft Co.'s Space & Communications Group in Los Angeles is forging ahead with the HS 393, a joint venture with the Japanese Communications Satellite Co. The HS 393 radiates anywhere from 2,200 to 2,600 W of power, compared with about 1,000 W for most satellites.

IT'S TAKEOFF TIME FOR SPEECH RECOGNITION, SAY JANET AND JIM BAKER

Jim and Janet Baker have worked in speech recognition long enough to know that predictions of a big year ahead come along every year. But the husband-and-wife team, which heads Dragon Systems Inc., a four-year-old company in Newton, Mass., takes a more conservative view. Next year will probably not see huge growth, the Bakers say, but it will be a pivotal year for speech-recognition technology.

"We will have the introduction of the first usable voicewriters," says Jim Baker, chairman and chief executive officer. The systems, in which the user speaks into the machine instead of typing, will be speaker-dependent, isolated-word products. They will include vocabularies of 5,000 to 20,000 words, he predicts. And at least one—from Dragon Systems—will cost less than $2,000.

This technology will be the basis for building a billion-dollar market in speech recognition, says Baker. "My opinion about why we haven't pushed through the knee of the curve [depicting the market] is that the technology wasn't what was needed by the consumer," he says. "In 1987, there will be the introduction of that technology."

JANET BAKER

JIM BAKER

The real key is how that technology is used. Dragon president Janet Baker says that most major companies now know that "to be competitive they will have to integrate high-performance speech-recognition capabilities." Product-design people have also become more sophisticated, she adds. Those people, Janet Baker believes, now understand the performance sacrifice required for speaker-independent systems and are choosing now to go for higher-performance speaker-dependent systems.

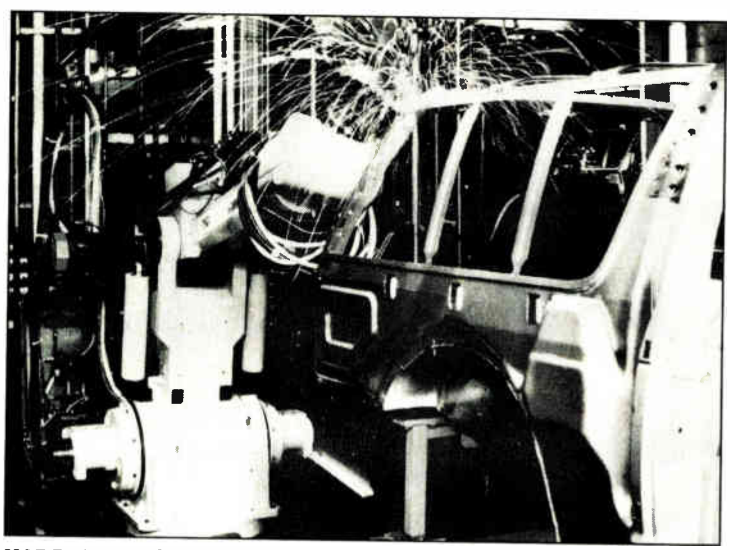
Given the technology advances and awareness among product planners, the Bakers say an important element for the growth of the speech-recognition market is still missing: applications. Single boards are being bought for development, they report, and some applications are likely to emerge in the next year. Nevertheless, Janet Baker says, "There are tremendous opportunities not being addressed."

The Bakers market their voice recognition systems independently and through arrangements with IBM Corp., Apricot Ltd., and other companies. Although bullish on upcoming developments in speaker-dependent speech systems, the Bakers are more bearish on user-independent continuous-speech systems, believing technology leaps are farther in the future. Says Jim Baker: "There aren't enough people concentrating on it." *–Craig Rose*

DATA COMMUNICATIONS

Advances in hardware and software will keep MAP networks forging ahead, and LANs for personal computers will see hot competition among varied technologies

by Robert Rosenberg



MAP READING. GM is testing carrier-band subnets, which use frequency shift-key modulation to send messages, for cell-level control.

The action in local-area networks will take center stage in data communications next year. The fast-developing area of factory LANs will move even faster, and the more-established field of LANs for personal computers will see a host of competing technologies mix it up.

Local-area networks for factory automation, especially those that adhere to the Manufacturing Automation Protocol, are pushing toward implementation. Hardware developments will drop the cost of connectivity to the MAP net; simplified software protocols promise to speed processing.

Innovation is also on the horizon in LANs for personal computers. Well-established personal-computer LAN makers are facing a technical challenge from a new breed of local nets. Low-cost networks based on RS-232-C and twisted-pair connections are offering the connectivity between personal computers that once only came from more-expensive networking schemes. The established vendors also must deal with the advent of the AT&T Starlan and with the fast-developing Token-Ring Network from IBM Corp.

The hottest spot for technical innovation in data communications is in factory-automation gear. The key MAP booster, General Motors Corp., started out looking at costly broadband radio-frequency gear, but now it is testing carrier-band subnets for cell-level control, which will drive down the cost-per-attachment to the net. These phase-coherent carrier-band subnets rely on frequency shift-keyed modulation for sending messages on a single pair of frequencies.

Motorola Inc. has a working version of a single-chip carrier-band modem, the MAP-compatible MC68194. West Germany's Siemens AG reportedly is developing a similar product—the SAB82511—and Intel Corp. is also said to have a single-chip carrier-band modem in the works. Delivery dates should be announced in 1987.

With manufacturing and process-control industries heavily committed to MAP, the next task for its backers will be to involve nonmanufacturing industries in MAP and in its sister protocol set for the office, the Technical Office Protocol.

"You've heard of islands of automation," says

says Charles J. Gardner, chairman of the U. S. MAP/TOP Steering Committee. "But our goal with this expansion is to prevent islands of corporations. We don't want to see another whole set of protocol stacks developed to meet the needs of various other industries."

Next year will also likely see more experimenting with the MAP Enhanced Performance Architecture (EPA) and MiniMAP protocol sets. Also known as collapsed architectures, both EPA and MiniMAP eliminate layers 3 through 6 of the MAP seven-layer set of protocols, which can help speed response times.

In personal-computer LANs, the established vendors are fighting back against new competitors by developing new technology. For example, Corvus Systems Inc., San Jose, Calif., is pushing to drive down the costs of its Apple II and IBM PC Omninet LANs. Crucial to this strategy is the Omninet controller chip—a CMOS part with the equivalent of 125,000 transistors—which NEC Corp., of Kawasaki, Japan, is ready to produce.

The trend toward developing specialized processors to handle LAN communications is likely to continue in the year ahead. "We've been doing application-specific integrated circuits like crazy," says Bob Metcalfe, founder and chairman of 3Com Corp. The Santa Clara, Calif. company has been using five ASICs for local bus-interface requirements for its EtherLink connections.

The drive by the established personal-computer LAN makers toward greater integration and increased functionality across a widely distributed network is aimed at a host of companies offering links among two to 10 IBM PCs or compatibles at a cost per connection of about $100. More than a half-dozen companies are already avoiding the costly coaxial cable connection needed to link up with Ethernet-type networks and the pricey silicon associated with the token-ring or Starlan adapter cards.

Instead, they are using such simple connection schemes as RS-232-C and twisted-pair serial-port connectors and developing networking software running under MS-DOS operating systems. Right now they are in the game with nitty-gritty functions such as file transfer and resource sharing, but in 1987 they probably will add increased functionality, such as electronic messaging. Though the speeds of these networks range from 19.2 kb/s to 57 kb/s—putting them well behind the nominal 10-Mb/s rate of Ethernet or the 1-Mb/s of Starlan—they are winning users away from the more established vendors.

Next year also should be the year that the long-heralded AT&T Information Systems Inc. Starlan LAN will become something more than a paper tiger. Starlan is a low-cost version of the IEEE 802.3 standard for a carrier-sense multiple-access network with collision detection. It substitutes twisted-wire pairs for coaxial cable. It is gaining important support from IC makers Chips & Technologies Inc., Semicustom Logic Inc., and Western Digital Corp. This should drive down the cost of interface boards in 1987.

For its part, IBM rounded out its token-ring LAN offering, adding functionality to its version of the IEEE-approved 802.5 LAN standard. Meanwhile, Texas Instruments Inc. has already cut 60% off the price of the five chips it offers to builders of IBM-compatible interfaces for the 4-Mb/s network. The price cut is probably in anticipation of the second-generation two-chip set, due no earlier than next spring.

GM'S KAMINSKI HAS MAP ROLLING ALONG

"People sometimes ask me how you make it in an organization as big as General Motors Corp.," says Michael A. Kaminski Jr. "And I always tell them that if you want to go off in a corner and hide, you can do it. But I also tell them that if you want to be recognized and do things and get out there and move and shake, there's plenty of opportunity for that here, too."

Kaminski, the Manufacturing Automation Protocol program manager at General Motors Technical Center in Warren, Mich., is living proof of his words. As the man who in 1982 took over GM's effort to make MAP a factory communications standard, he has done his share of moving and shaking.

Kaminski's hand-picked staff of three has swelled to a cadre of 40 communications and automation specialists. Pilot MAP networks are operating at 10 GM factories. More important, the MAP effort has gained widespread industry support from an estimated 1,500 companies worldwide.

The 53-year-old Kaminski became interested in computers in the late 1950s at Burroughs Corp. in his native Detroit. While there, he earned an MBA from Wayne State University, where he also earned his bachelor's degree in industrial engineering. He then worked at several companies, developing automation systems. He joined GM in 1969 as a senior project engineer.

Kaminski compares the MAP development effort to rolling a huge rock over a hill. "We've come over the hump in roughly the last six months, with the successful culmination of the Autofact '85 MAP demonstration [*Electronics*, Nov. 11, 1985, p. 16], and now we're on the downhill side." But challenges remain. As MAP gains momentum, Kaminski sees a complex job ahead in managing the diverse interests and requirements of a growing legion of users, vendors, and standards-setting organizations around the world.

MICHAEL A. KAMINSKI JR.

"There's a definite path that we want the rock to follow on the downhill side. But the rock still could go out of control fairly easily," Kaminski warns. "And if you don't watch out, then the damn thing could just run right over you."–*Wesley R. Iversen*

FROM EARTH

Voyager 2 is on a mission to explore the outer solar system, with the help of RCA High-Rel devices.

On August 20, 1977, Voyager 2 set off on one of NASA's most ambitious journeys. Its goal was to explore Jupiter, Saturn and then the limits of the solar system, sending back information along the way.

Earlier this year, the satellite passed a milestone when it flew within 50,600 miles of Uranus, sending back extremely high-resolution photos of that hitherto unexplored planet.

Now Voyager is hurtling towards its next scheduled rendezvous—with Neptune, nearly 2.7 billion miles from home. After that, this extension of our civilization will head for the edge of the solar system.

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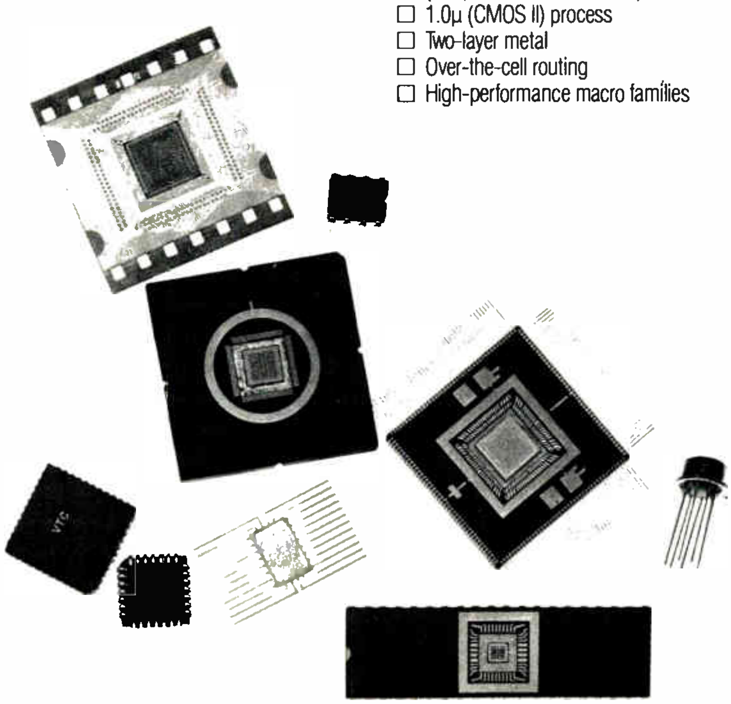

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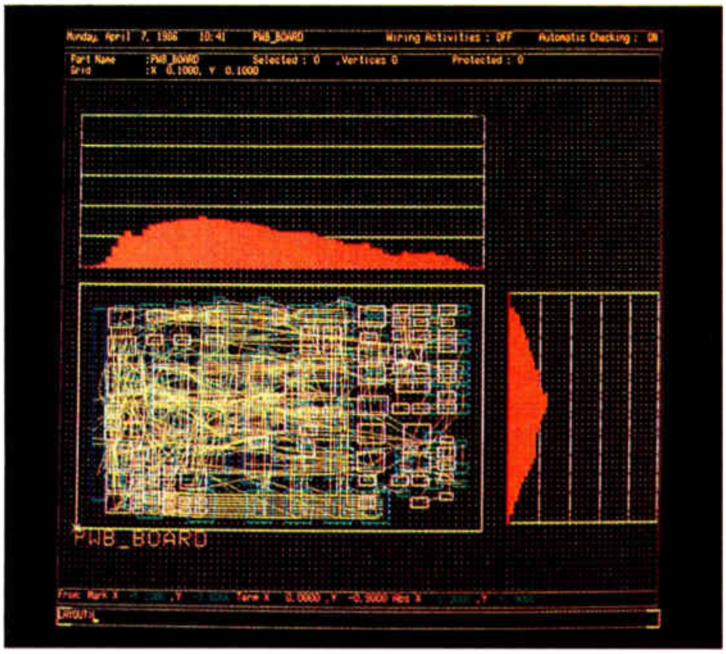
COMPUTER-AIDED DESIGN & ENGINEERING

In hardware design, the spotlight is shifting from digital to analog tools; in software development, computer-aided engineering will start to expand mightily

by Jonah McLeod



TRAFFIC COP. Histograms on this Mentor Graphics work station's display identify areas of maximum wiring congestion.

Today there is an imbalance in the quality and quantity of computer-aided engineering tools for developing electronics designs. Far more systems exist for digital than for analog design, and too few are available for software design. But in the coming year, manufacturers will be working to correct that imbalance, devising improved gear for analog design and a bevy of computer-aided software-engineering programs.

"To date, there has been no board or system-level analog design tool," says Larry Jacob, president of Analogy Inc. in Beaverton, Ore., which is working on a powerful analog simulator. "Yet 80% of all printed-circuit boards and 50% of all custom integrated circuits contain mixed analog and digital elements." Moreover, hardware represents only part of most projects. Software accounts for 50% of most design projects, and the percentage is growing. New tools are needed for software engineers, too.

Beginning next year, CAE tools will emerge that provide analog design and software engineering with gear as sophisticated as that being used in digital design. Simulators will replicate the functions of analog design before it is ever put into hardware, while computer-aided software engineering tools will improve the flow of work in one of the least productive parts of a larger design effort: software development. In 1985, the total simulation software market was worth less than $100 million, according to Technology Research Group in Boston, Mass. The group expects the market to reach $250 million in 1988.

"Analog design is growing in importance to CAE designers," says Frank Costa, general manager of the design and analysis division of Mentor Graphics Corp. in Portland, Ore. "They want to design in mixed-signal environments in which they are able to simulate both analog and digital components of a circuit together."

To meet their needs, a new breed of simulators is being developed, among them a unit from Sierra Semiconductor Corp. of San Jose, Calif. (see p. 60). Not only does the tool simulate the analog circuit behavior, it also functionally simulates analog and digital together, unlike the lower-level Spice circuit simulation done today. Other companies are also working on analog simulators. According to Analogy's Jacob, these simulators "will be able to model an analog circuit without knowing what the actual circuit implementation is."

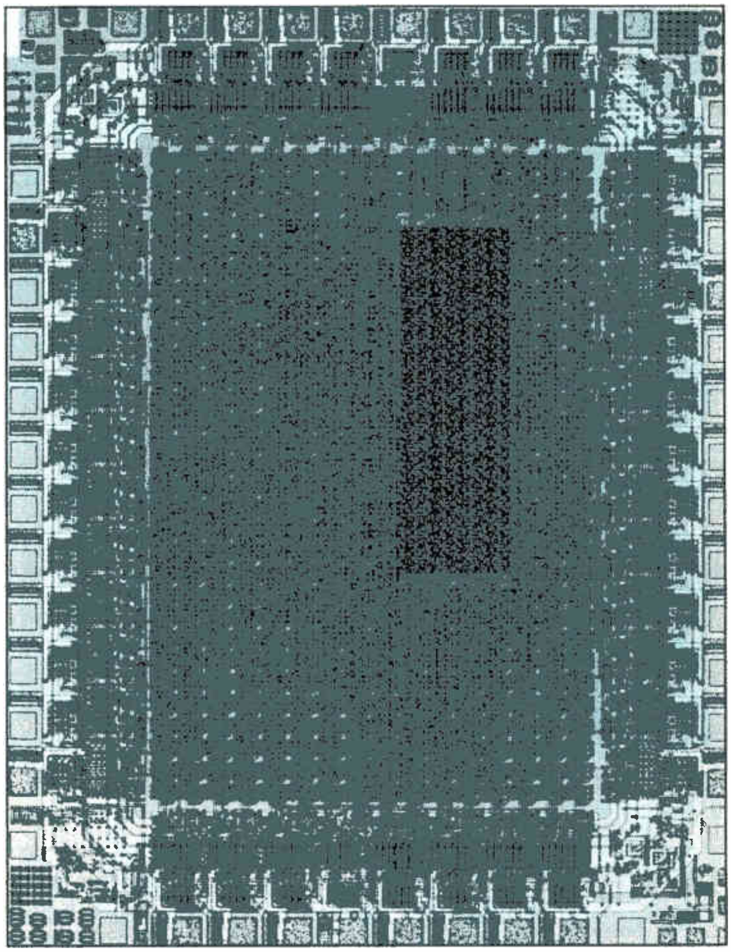
One development that will facilitate functional analog and digital simulation is the advent of mixed-signal environments. "The advantage of behavior models is that the simulation algorithm is event-driven," says Jim Caldwell, senior development engineer at Sierra. "As a result, simulation time will grow proportionally with circuit complexity." By contrast, simulation times on analog-circuit simulators such as Spice tend to grow exponentially, because the simulation is attempting to recreate detailed device functions rather than larger circuit behavior.

As with the increased use of analog simulation, the next three years will see more digital logic simulation of components on personal-computer boards. "Despite the widespread availability of simulators, board designers have not simulated their circuit design as extensively as have IC designers," says Michael Turner, director of marketing at Logic Automation Inc., Beaverton.

One reason is that these simulators are hard to use. Also, the designer must create models of the very large-scale integration components contained in the board's design, a job most are unwilling to do. Companies such as Logic Automation, Quadtree Inc., and all the work-station vendors provide some models. But the real impetus for large model libraries will come when semiconductor makers such as Advanced Micro Devices Inc. and others begin making models available as soon as the chips come to market. AMD, in Sunnyvale, Calif., is already aggressively taking this tack in conjunction with Logic Automation.

In the design of application-specific ICs, silicon compilation will begin to come closer to fulfilling its promise of true automatic circuit generation from a specification developed by the engineer. Warren Snapp, vice president of engineering at Seattle Silicon Technology Inc., Bellevue, Wash., explains. "In theory, humans should be able to produce a more compact design than a compiler, given unlimited time and resources. However, time and cost are constrained. With a compiler, you can compile a complex chip and have it placed and routed in an afternoon." The company's proprietary "dynamic compaction" compilation technique produces the smallest cell in silicon to date. Snapp says that as work progresses on the silicon compilers, it will soon be impractical for a designer to spend the time designing a circuit from the ground up.

Perhaps the most costly part of any design is software development. "It costs $70 for every line of code written in the design phase of a major software effort," says William Sharon,



NO CHANNELS. This chip was developed using California Devices' channelless gate array router for maximum compaction.

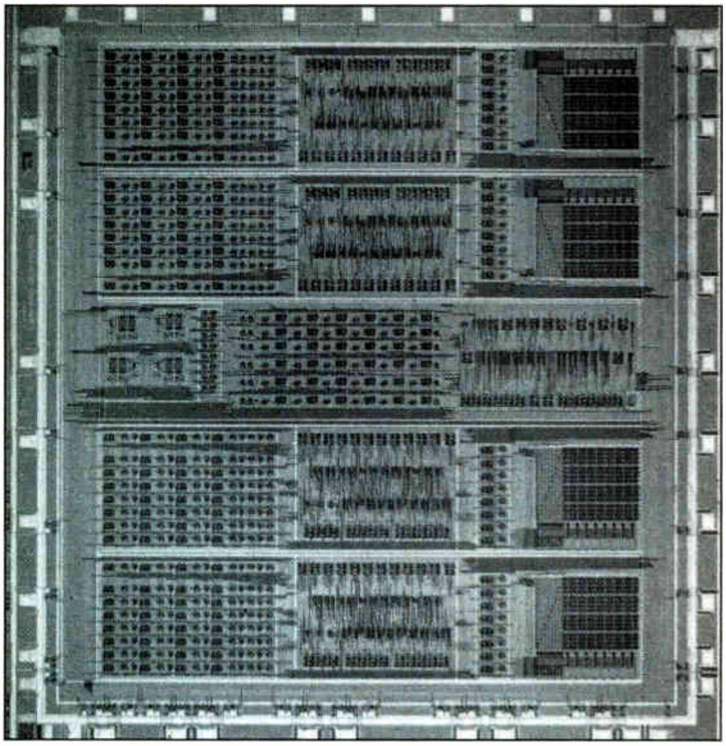
marketing manager for software-design environments at Tektronix Inc., Beaverton. "If the code has to be changed after the product is in the field, it costs $4,000 per instruction."

But cost is not the only reason for the onrush of new software engineering tools. Program size is another factor. Gordon Reid, marketing manager for development systems at Intel Corp. in Hillsboro, Ore., says, "In 1978 the typical microprocessor program was no more than 4,000 bytes long. Now, programs range from 200-K bytes to 500-K bytes in size."

According to Intel's research, the ideal design system would enable a project manager to specify an application with one tool. Programmers would then write the software, and another tool would automatically evaluate the code to see that it meets the specs.

The design process consists of analysis, design, prototype, code, and test, and William Sharon at Tektronix says these steps will one day be integrated. Essential to this effort, he says, will be two things: a central data base used with code, test, and integrating tools, as well as integrated programming environments with an incremental compiler.

Just as the ASIC designer has silicon compilers



VERSATILITY. Seattle Silicon's compiler can now produce mixed analog and digital designs like this.

to automatically generate a laid-out circuit, so in software design will automatic code-generation and high-level product-generation tools help in creating the code. Eventually, the programmer will specify a function, and the generator will produce code that implements it. However, such functionality is three to five years away.

New tools that will find their way into the design process in the next five years will be those providing complete project management for hardware and software. Up to now, designers have focused their attention on providing computer-aided software-engineering tools that control the production of software. "CASE provides configuration management but falls short of managing the total design process," says Arthur Fletcher, president of Sherpa Corp. in Milpitas, Calif.

The tool Fletcher envisions will control every piece of documentation generated during the course of a project and will maintain that documentation in a central data base. Any change made anywhere in the project will be immediately reflected in the data base.

In addition, hardware designers will be given new planning tools that will give insight into the costs, power consumption, and size of designs before work is actually begun. Typical of such tools is the Design Assistant from VLSI Technology Inc. of San Jose, Calif. (see p. 53). It gives an ASIC designer alternative implementations of a proposed circuit based on preliminary data entered by the designer: a block diagram with input and output lines specified, a schematic of an existing pc-board design, and so on. Similar planning tools will provide software designers with the ability to plan the partitioning of a design comprising hardware and software. "The designer splits up the hardware and software components and must wait until design integration time before he realizes that he needs to put some software function in hardware to make it meet performance spec," says Sharon. A planning tool interacting with a hardware and software simulator would allow this determination to be made early in the cycle.

AUTOMATING THE DESIGN BACK-END

At the back end, automatic place-and-route tools will completely lay out designs on PC boards and ICs more efficiently than is possible with manual intervention. Where both have traditionally been laid out with routing tools based on early place-and-route software developed for pc-board layout, a new generation is being developed specifically for ICs.

Typical of the new place-and-route capability is the Wise II gate-array place-and-route tool from California Devices Inc. of San Jose. Unlike the conventional channel router, Wise II is a channelless router that uses no specified routing channels but rather places gates as closely together as possible. It uses the two layers of metal common on the current generation of gate arrays to connect up the gates.

"In the next year to 18 months, this capability will be extended to accommodate gate arrays containing large standard-cell blocks [such as register, counter, and arithmetic unit] in among the sea-of-gates," says Martin Harding, director of strategic marketing at CDI. Already VLSI Technology is offering such an array.

The next one to three years will see gate-array suppliers shifting from channelled to channelless array architectures. "Most gate-array vendors bought and developed channelled routers to lay out their arrays," says Harding, "and they are now in the process of modifying their software to accommodate the channelless architecture in order to get the high density required to remain competitive in the semicustom market."

In standard and macro cells, placement and routing until now has been an interactive task. The designer lays out the larger blocks, and the software makes an attempt to route them. Often, the designer might interact with the router to facilitate the process. Recently, Seattle Silicon released a place-and-route tool that for the first time guarantees automatic layout and the routing of both standard blocks and the company's own silicon-compiled macro blocks. The product is a precursor of the next-generation place-and-route tool. "Improvements were made on the router to handle dual-layer metal," says Snapp, at Seattle Silicon. "In addition, the tool will be able to handle three-layer metal when it first appears."

But if any one feature can be singled out as likely to have the biggest impact on the design process, it's automatic placement. "In the next few years, our placement algorithm will become so much better than manual placement that it will no longer require an expert layout designer to get the most efficient chip," says Snapp. "At that time, silicon compilation will begin to appeal to the system designer who may not be familiar with IC layout." Another function that will soon be provided by silicon compilers is the ability to recompile circuits designed in one technology, say CMOS, into another, like GaAs. Richard Oettel, chief scientist at Seattle Silicon, says the company has demonstrated this conversion and can also recompile into silicon-on-sapphire and bipolar ECL. Silicon Compilers Inc. of San Jose expects to be able to convert into silicon-on-sapphire as well.

IMPROVING DATA FLOW

Alongside the group of upcoming tools designed to increase productivity, there is also some movement toward standardizing the data that moves throughout the design process. CAE suppliers and customers are proposing two file-format standards: the Electronic Design Interchange Format, supported by the Electronic Industry Association, and the American National Standards Institute's Initial Graphics Exchange Specification. This movement will help solve the problem of dissimilar data bases produced by different CAE software vendors. As it stands now, the schematic captured on one CAE software package cannot be run easily on a simulator from another manufacturer.

Part of the impetus for this standardization comes from the Department of Defense. "The DOD is starting to specify that design data be specified in a high-level hardware description language," says Mentor Graphics' Frank Costa. He thinks this is an indicator of a much larger trend to a more open architecture in design tools in general.

"Today, the design tools are linked together in a linear fashion," he says—that is, a file created by schematic capture is passed on to the simulator, and then that file goes to the layout software. "The new way will be built on a centralized data base." The designer may have several windows on a work-station screen for each tool, with a change in a file in one window immediately reflected in the rest. Before such an open system can be built, work-station vendors must open up their data formats, so that software vendors can create tools that are compatible with the work-station data. Costa thinks some level of standardization will occur next year.

WHY WILLETT SEES A BIG CAE ROLE FOR INTEL'S 80386

Kenneth G. Willett is optimistic that the promise of computer-aided engineering—a work station on every engineer's desk—will be fulfilled. Willett, advanced product director at Mentor Graphics Corp. in Beaverton, Ore., sees the advent of the work station built around the 80386 microprocessor as helping CAE deliver on that promise.

CAE hardware suppliers have made several attempts to produce the appropriate work station for the CAE market, but Willett believes those based on the 80386 will approximate what the market wants. "The $50,000 Apollo was not the machine to put on everybody's desk, and the $6,000 IBM PC AT was not the right machine either," Willett says. "We as equipment suppliers are beginning to hone in on a computer in the $10,000 price range that has a high-resolution display and an 80386-class microprocessor inside."

KENNETH G. WILLETT

He believes that the availability of 80386-based computers, rather than their architecture, makes them particularly well suited to produce this ideal CAE work station. "Everyone currently making the PC AT will make a 386 machine," he says. "So people will be able to buy the computer at a computer store, which is not the case with the Apollo or Sun work station, although all three will be in the same price range."

The wide variety of available software will also help make the 80386-based work station the universal system. Anything that runs on an 80286 will be available for the 80386, Willett says. Beyond that, the 386 machine will probably also offer the Unix operating system and associated languages, as well as a large virtual memory. Thus, software written for work stations will fit the 80386-based system.

"I think the 386 machines will have software that you can buy for a 32-bit Unix work station and most of the software you can buy for a PC," Willett says. "For those engineers who dream of being able to do spreadsheet and word processing on the same desktop computer they use for schematic capture and simulation, the 386 machine is going to be the ideal environment."

However, Willett says, the new computer systems will not totally replace existing work stations. Instead, there will be a two-tiered market: the customer who has never bought any CAE equipment will prefer the 386-based work station. "People who are buying work stations today are going to continue buying them." he says.

"The 386 will break down the resistance of buyers who haven't felt comfortable buying Apollo or Sun equipment. If the system does not work out as a design-automation system, it can always be used for word processing and spreadsheets."

Willett says the 386-based systems will have an impact on two types of CAE vendors: those who are abandoning proprietary hardware, and those who have profited little from PC-based systems. The latter will quickly make the higher-performance system their main platform, since they will be able to increase profits by charging more for their software. *–Jonah McLeod*

TEST & MEASUREMENT

Automatic test equipment is entering the ASIC age; test generation is getting easier, and simulators that handle mixed analog-digital ICs are appearing

by Jonah McLeod

The application-specific integrated circuit is exerting a strong influence on instruments for test and measurement. Moreover, many of the requirements for ASICs also apply to standard ICs. ASIC parts require higher pin counts—growing to more than 250 pins next year—and faster clock rates, edging up from 10MHz to 20 MHz. And 50% or more have both analog and digital components on board. ASICs differ most significantly from standard parts in production runs: where the production of a standard part can hit millions a year, ASIC typically runs less than 100,000 a year.

To cope with this testing demand, automatic test equipment is being scaled down in size and price. The new LT1000 from Tektronix Inc., of Beaverton, Ore., for example, starts at $650,000, yet offers test capability up to 250 pins. Typically, ATE for standard parts costs from $1 million to $5 million.

"ASIC foundries are smaller companies with tight budgets and not a lot of room to accommodate a roomful of testers for checking ASICs," says Al Perry, vice president of marketing at Semiconductor Test Solutions Inc., Santa Clara, Calif., which makes a $700,000 250-pin system.

Another system, built by Cadic Corp., is a 256-pin tester selling for $175,000. The Beaverton company's system is extremely flexible; all pins, for example, can be bidirectional and switched from input to output on the fly. Having all pins configurable means that the tester can easily accommodate a wide variety of devices.

"The characteristic of ASIC designs is that they are unique for each production run and there are no more than 100,000 or so parts to test for any given design," says Dan Dunatchik, engineering project manager of the Tektronix semiconductor test-systems division. "Test generation becomes a major bottleneck in the life of an ASIC part." To solve this problem, the company is now readying its Arnold software for introduction next year; it claims the program will cut test-generation time by a factor of five. Arnold

PRECURSOR. Architecture of Teradyne's A370 analog VLSI tester anticipates one-pass analog and digital testing of mixed-function chips.

simplifies the programming required to configure a test system: the designer merely tells the system that a pin is to have a certain dc level; the system does the rest. Future versions of such products will simply require the engineer to answer a few questions about the circuit to be tested, after which the system will generate the pattern itself.

Many other companies will be working on a faster and simpler generation of tests for 1987. "Test generation is being made easier by software that converts data from the computer-aided-design system simulator and converts it into test vectors for the test system," says Gene Roth, marketing manager at GenRad Inc., Concord, Mass. This trend began to emerge this year

A software package called HiPost does the job on the GenRad GR180 family of semiconductor test systems. With HiPost, files can be transferred over Ethernet directly to the test-program generation station. "Most companies have not networked their testers with their design labs," says Leif Rosqvist, president of Test Systems Strategies Inc., Beaverton. "Without networking, simulator output files are moved from lab to factory via nine-track magnetic tape."

In addition to improving communications, companies must enhance the test data itself to shorten program-generation time. Test Systems Strategies is about to address this problem. "We intend to make the transfer of data between lab and factory two-way. Information about the testing environment can be transferred back to the design engineer so he can design his component to be more easily tested," Rosqvist says. Ordinarily, an engineer who has a tester that cannot replicate a timing pulse produced by the simulator has to call the designer to determine how to solve the problem. In the new approach, the designer will know the tester cannot replicate the pulse; he can devise an alternative when he first creates the simulator data.

One characteristic of ASICs that dictates different testing methodologies is the package. "Because of their large pin counts and relatively low volume, these circuits require packages that are two and three times the price of the die," says Curt Stein, marketing product-line manager in the Tektronix Accessories Division. "With standard parts, only the parametrics of circuits on a wafer were tested. ASIC manufacturers want to test functionality of devices on the wafer before the parts are cut and put into packages."

TESTING MIXED-SIGNAL DEVICES

Another step forward in ATE that owes much to developments in ASICs is the advent of mixed-signal simulators that can functionally simulate the operation of both analog and digital components. Test-system architectures will have to change to accommodate this new type of test data. In the past, the manufacturer testing mixed-signal chips would first test the digital component on a digital tester and then test the analog component on a separate tester. The next approach was to combine a separate digital and analog tester in the same chassis. By next year, the two testers in the same chassis will become one test system.

A precursor of this new architecture is found in the A370 from Teradyne Inc. of Boston. "The vector bus inside the system integrates the digital and analog equipment," says Michael Bradley, marketing manager of analog LSI test systems. "It synchronizes sources and responses and allows software to orchestrate the execution of tests." Future generations will be refined to enable full functional testing of the complete chip in one pass.

TO B.J. MOORE, SPEED MEANS FAST HARDWARE

In an era when software designers command increasing respect and royalties, B. J. Moore is an unabashed hardware enthusiast. "No matter how much you talk about architecture," Moore says, "if you want high speed, you run the hardware as fast as you can."

The new minisupercomputers, superminis, and new gallium arsenide-based systems are pushing to even higher speeds, Moore notes, and the equipment to test them must be even faster.

"A 500-MHz clock gives you a resolution of 2-ns ," Moore says. "That's a crude look at a 5-ns device and no information at all on a 1-ns ECL circuit."

B. J. MOORE

More than a decade ago, Moore broke new ground in instrumentation by developing the first logic timing analyzer, the Biomation 810-D, winning him a share of the 1977 Electronics Achievement Award [*Electronics*, Oct. 27, 1977, p. 82]. This year, as president of Outlook Technology Inc., a Campbell, Calif., startup, Moore is grooming a new logic timing analyzer for introduction at Wescon next month.

Although he is not talking yet about the specifications of the new instrument, Moore hints at performance in the multigigahertz range, adding: "We will be able to make several kinds of measurements never made before."

The new instrument was designed by Outlook Technology founder Curt Blanding, 43, a onetime colleague of Moore's at Biomation Corp. in Santa Clara, Calif. Most of the fledgling company's personnel are also Biomation alumni, who founded Outlook Technology and recruited Moore, an early investor, as president a year ago.

Moore, who left Biomation in 1980, 18 months after it was acquired by Gould Inc., says he's glad to be in instrumentation. Unlike computers or semiconductors, he says, "It's a very sane business. People don't get hyped, they understand what they are doing, and they don't expect the impossible." *–Clifford Barney*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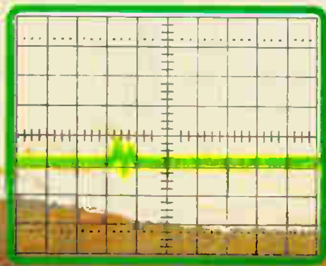

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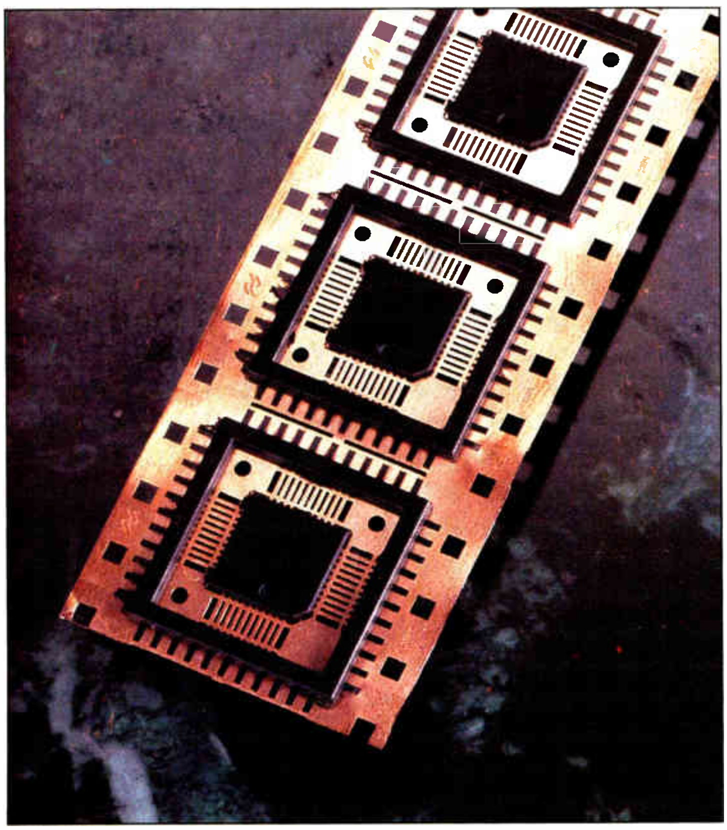
PACKAGING

IC packaging is changing fast, as leaded ceramic and fine-pitch chip carriers go commercial, two Japanese packages debut, and tape-automated bonding surges ahead

by Jerry Lyman

Driven by the dual stimuli of very large-scale integration chips and the Defense Department's Very High Speed Integrated Circuits program, the world of electronic packaging is in a state of flux and probably won't settle down for quite a while. IC packaging is again in transition, with leaded ceramic and fine-pitch chip carriers making their debuts in commercial products. At the same time, two packages developed in Japan—the ZIP (zigzag in-line package) and the 70-mil dual in-line package—are making waves in the U.S. And a major effort is under way to make the premolded leaded chip carrier meet the environmental needs of the military.

In another area, tape-automated bonding is fast becoming the favored method for packaging extremely high lead-count devices. The frame width of TAB tapes is rapidly growing, and molded and encapsulated TAB is adding to the potential of this automated technique.



TAPE PAK. National Semiconductor's Tape Pak is a small molded package, whose leadframe is a copper tape, with gull-wing leads on 20-mil centers.

LEADING ON

Until recently, the leadless ceramic chip carrier was the IC package of choice for military-aerospace uses and for some critical computer applications that required a hermetically sealed package. Leaded ceramic chip carriers were not available except on a custom basis. But with carrier lead counts rising as high as 224, the bloom has started to go off the leadless types.

The reason is that the leadless ceramic carrier has an inherent thermal mismatch with conventional printed-circuit boards. It must be used with special thermally compensated boards or, in the military environment, the solder joint between carrier pads and personal-computer board pads will crack [*Electronics*, July 10, 1986, p. 93]. In carriers with more than 68 input/output pads, there is considerable doubt whether even compensated boards will keep the solder joints from cracking under thermal stress.

Because of this difficulty, high-lead-count leaded ceramic chip carriers are now starting to appear commercially. Intel Corp.'s military division, for example, is supplying certain microprocessors in a 68-lead, 4-sided ceramic flatpack with leads on 50-mil centers. The compliant leads take up the thermal strains and allow the use of standard pc-board laminates.

Until recently, only Kyocera Corp. and NTK's Technical Ceramic Division, Richardson, Texas, furnished this type of package commercially, but now Jade Corp., Southhampton, Pa., has just entered the game with a family of 20- to 84-lead leaded ceramic carriers with leads on 50-mil centers.

Whether leaded or unleaded, an increase in I/O count means a larger carrier. To counter this, package manufacturers are building ceramic chip carriers with a pitch finer than the normal 50-mil pitch. Units are becoming available in 25-, 20-, and 10-mil pitches, most of them aimed at VHSIC chips but some appearing for the first time in commercial ICs.

For example, Integrated Device Technology Inc., Santa Clara, Calif., is already putting its CMOS multipliers and multiplier-accumulators in a leadless ceramic chip carrier with 68 pads on 25-mil spaces. Supertex Inc., Sunnyvale, Calif., is packaging its high-voltage drivers in an 84-lead Quad Cerpack (a ceramic glass package similar to a CERDIP) with gull-wing leads on 25-mil centers.

Commercially, only Jade and Amp Inc. are supplying fine-pitch carriers in the U. S. Jade offers high-lead-count ceramic four-sided flatpacks with leads on 25-, 20-, and 10-mil pitches. Amp, of Harrisburg, Pa., has developed a novel single-layer, fine-line carrier based on electroplating 1-mil-thick copper traces to a ceramic substrate. Using this technique, the company has manufactured prototype carriers with 320 pads on 10-mil centers [*Electronics*, Sept. 18, 1986, p. 46].

The fine-pitch carriers will pose increasing problems for the pc-board and socket industries struggling to interconnect and align with these densely packed pad or lead patterns. With the advent of faster bipolar and CMOS logic and the debut of GaAs digital chips, carriers with better transmission-line characteristics should become increasingly available in the next few years.

While the spotlight is on the fine-pitch carrier, two plastic packages developed in Japan, the ZIP and the Shrink-DIP, have become available in the U. S. The ZIP is a single in-line package with staggered leads on 50-mil centers. Used mainly for housing semiconductor memories, this package has the packing density of the single in-line package but may be mounted on 100-mil centers. It has been adapted by several Japanese companies, including Fujitsu Ltd., Hitachi Ltd., and Mitsubishi Electric Corp. And at least one American company company, Micron Technology Inc., Boise, Idaho, is already using it to package high-density memory chips.

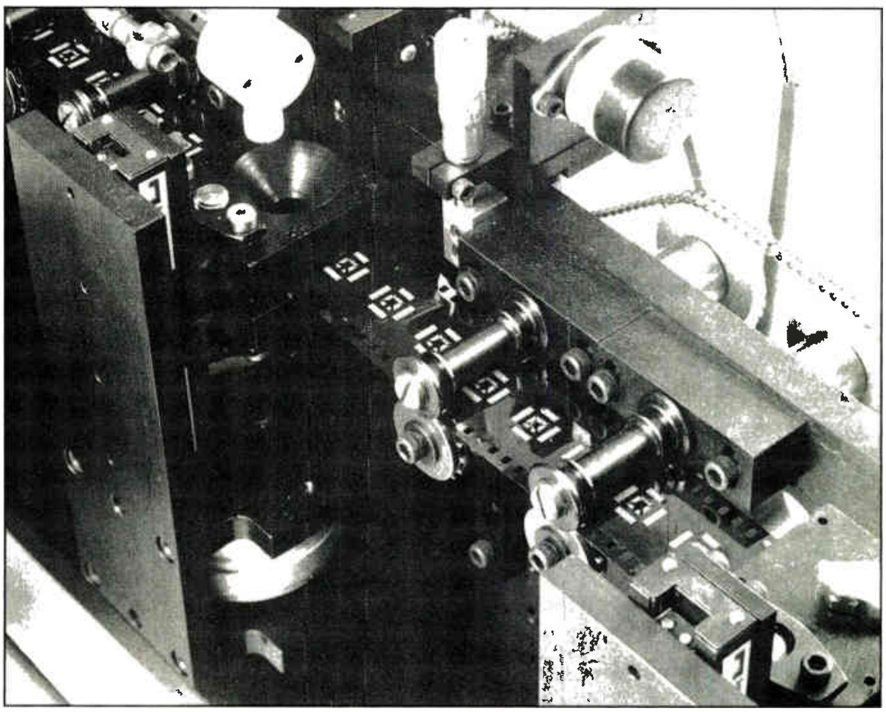
Another plastic package that may migrate to the U. S. is what is called the Shrink-DIP. This unit has leads on 70-mil, rather than 100-mil, centers, which cuts DIP size by about a third and causes only minimal assembly changes over its big brothers.

A potentially significant development in the world of plastic packaging was the formation last April of an IEEE task force, comprising about 20 electronic system houses, to test premolded plastic chip carriers protected from humidity by silicone gel to see if the devices could meet military specifications. If the program is successful, it could help the military cut the costs of IC packaging by eliminating the use of leadless ceramic chip carriers.

Jack Balde of Interconnection Decision Consulting, Flemington, N. J., the task-force chairman, reports that the group is up and running, with plans to test six different types of silicone gels. Next month, the task force will present a progress report at the sixth annual International Packaging Conference in San Diego.

After about 15 years as an underdog, tape-automated bonding has finally found its place in U. S. electronics. The TAB renaissance has shown up in several ways.

For one thing, the makers of VHSIC and VLSI chips agree that tape packaging is the best way to handle, test, and even burn-in multileaded complex VLSI chips. A number of VHSIC suppliers—among them Honeywell, National Semiconductor, and Texas Instruments—are turning out tape-bonded chips in ceramic chip carriers, while



MESA PAK. Mesa Technology uses this machine for reel-to-reel encapsulation of TAB-bonded devices. Encapsulation prevents edge shorting and fatigue stress on the bonded device.

TI and Honeywell are supplying commercial VLSI chips in the same type of assembly.

Because of the large surface area of VHSIC and VLSI chips, tape widths are growing. The early "jelly beans" (14- to 16-lead types) used 14-mm tapes. The latest generation of TAB is on 35- and 70-mm tapes, while 105- and 140-mm tapes loom on the horizon.

Two of the more interesting TAB developments of the year are encapsulated and molded TAB. West Germany's Siemens AG and a number of

Borrowing a Japanese technique for producing tape-automated bonding, Mesa Technology covers chips on tape with any encapsulant from epoxy to silicone gels

Japanese firms have been using TAB chips covered with an encapsulant in chip-on-board applications for years. Now, under license to Siemens, Mesa Technology of Mountain View, Calif., is supplying encapsulated chips on tape in the U. S. Mesa uses a Siemens machine to cover chips on tape with a customer's requested encapsulant—frequently epoxy, but silicone gels are starting to be used as well.

Meanwhile, National Semiconductor has developed its own novel method for producing a tiny fine-pitch molded package based on TAB and known as the Tape-Pak process. Tape Pak is centered around a bumped single-layer copper tape. Chips are mass-bonded to this tape, and then the package and a test ring are molded to each tape frame. In effect, the copper tape is the lead frame for a mini-package.

The package leads are on 20-mil centers, while the leads on the test ring are on 50-mil centers. After testing, the ring is excised, leaving a small molded package. With Tape Pak, packages can contain from 28 to 300 leads. Its small size (80 to 124 leads in a unit 700 mils on a side) provides significant electrical performance improvements over competitive packages.

TAB still has plenty of room to grow in other areas. For example, 3M Co., Austin, Texas, and IMI Corp., Cherry Hill, N. J., are both involved in work with multilayer tapes. This approach will increase the interconnection density of TAB and may yet be needed for the monster chips that are now in the works.

And one of the more important long-term developments will be multichip TAB, says Jack Hullman, Mesa Technology's vice president of sales. In this process, multiple chips are bonded to a single frame of a tape and electrically interconnected on the surface of the tape—a sort of miniaturized flexible circuit.

With the fine-line capabilities that the tape suppliers have developed, tape frames with two to seven chips are no problem. The first application of this technology was probably in smart-card electronic circuitry, such as the work done at IMI. However, the mini-tape substrates can be mounted to all types of motherboards, as shown by a joint 3M-Honeywell program where tapes were attached to porcelain-coated steel, alumina, quartz, and epoxy glass. This technique could provide a tremendous size reduction for modular assemblies of all types.

FOR A STRAIGHT ANSWER ABOUT INTERCONNECTION, ASK BALDE

When it comes to what's new in printed-circuit boards, chip carriers, or interconnection technology in general, Jack Balde has the answer. Balde, the one-man show behind Interconnect Decisions Consultants, which he runs out of his home in Flemington, N. J., has been a leading expert on electronic packaging technology for almost 20 years.

Balde is outspoken on just about anything to do with interconnection technology. His advice on using leadless chip carriers: don't. "They've got to go," he says. "There's more misunderstanding of the performance of leadless chip carriers than any other area of the technology." Are ceramic packages worth the extra costs for production? "Get rid of ceramic," he says; "too many problems."

JACK BALDE

But Balde, a rotund man who refuses to divulge his age (lest his customers write him off as over the hill, he says), is not just a talker. He is a technology driver, whose expertise lies in tackling serious problems.

Balde organized the Compliant Lead Task Force, a group of experts bent on eliminating leadless chip carriers in favor of leaded carriers with pliable leads. Balde promises to cause a stir when he releases the group's findings next month at the International Electronics Packaging Conference in San Diego. Likewise, it was Balde who established the IEEE Gel Task Force, a group investigating premolded plastic chip carriers protected by silicone gel as a replacement for leadless ceramic chip carriers.

One of the founders of the International Electronic Packaging Society eight years ago, Balde served as its chairman from 1984 to 1985. He has won numerous awards from that organization and the Institute of Electrical and Electronics Engineers, and while he was at AT&T's Bell Laboratories, he established the interconnection technology group in Whippany, N. J. [*Electronics*, Oct. 28, 1985, p. 57].

Balde's list of past and present clients reads like a who's who in electronics: IBM, Sperry, DuPont, and AT&T are a few of them. He says he has advised W.L. Gore & Associates Inc. to use its Gore Clad material in printed-circuit boards [*Electronics*, June 2, 1986, p. 21], and he says he also encouraged DuPont to get into that business. At any given time he has from 10 to 20 firms on retainer, with more on a waiting list. "There are only two kinds of consultants," Balde says. "Those that are too busy and those who don't have enough to do." *–Tobias Naegele*

MANUFACTURING

Computer-integrated manufacturing is finally making an impact on electronics, and artificial intelligence on the factory floor is beginning to gather steam

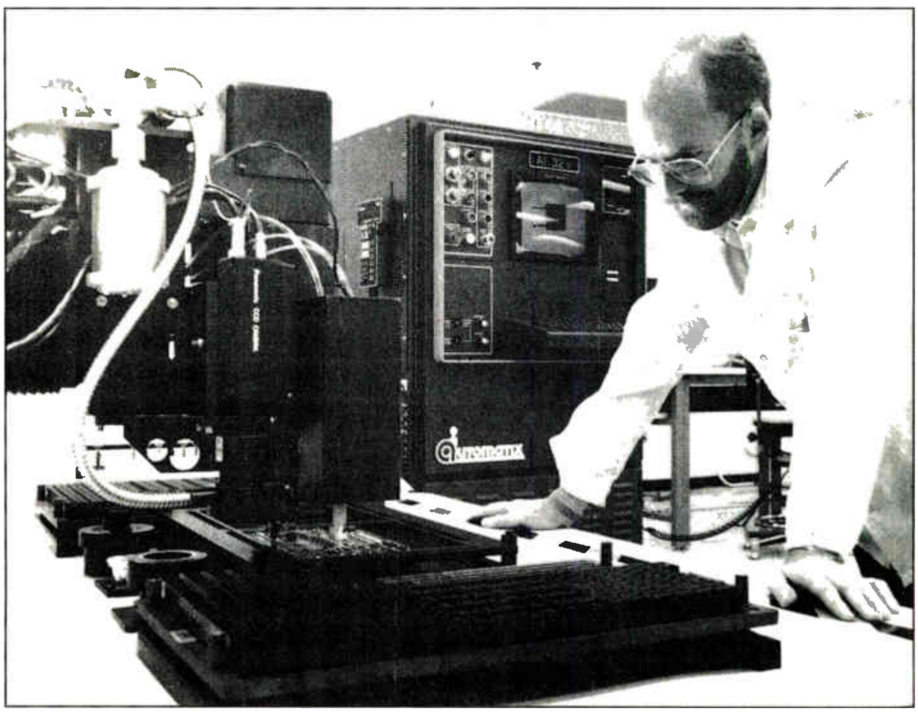
by Jerry Lyman

Computer-integrated manufacturing is finally beginning to trickle down from the automotive and aerospace industries to electronics manufacturing. At the same time, artificial intelligence, often considered an esoteric technique, is appearing on the factory floor, in the machine shop, and even in the scheduling room, generally in the form of expert systems. And flexible manufacturing systems—one of the building blocks of CIM—are showing up in integrated-circuit assembly.

According to a recent industry survey, only about 130 U. S. companies have full-blown CIM programs, with the great majority of them concentrated in the automotive, industrial, and aerospace industries. From that base, CIM is spreading out—many of the aerospace companies that have electronics capabilities, for example, are installing CIM-controlled production facilities. Rockwell International Corp. is one of them; the company now has an automated manufacturing cell for assembling surface-mounted boards and an Automated Material System for stockpiling parts at its Defense Electronics Operations plant in Anaheim, Calif.

Among the relatively few electronics firms engaging in a large-scale CIM effort is Tektronix Inc. The large Beaverton, Ore., instrument maker has been working on manufacturing integration since the late 1970s, first with computer-aided design and gradually, over the last two to three years, linking CAD to computer-aided manufacturing.

This CIM setup is typical of what will be standard in the future—a network controlling physically remote resources. The company's divisions are widespread; a production design group in Wilsonville, Ore., for example, is linked by CIM with a printed-circuit fabrication facility in Morris Grove, 50 miles away.



AUTOMATED ASSEMBLY. Rockwell's manufacturing cell uses robotic equipment to dispense adhesive and place parts.

Each of the five major Tektronix production groups has its own CAD system, all of them interconnected across a company-wide microwave network. The CAD data is fed through a shop-floor gateway to a Manufacturing Automated Protocol network. From there, the data goes to a cell controller that interfaces with either controllers on the shop floor or intelligent interfaces for semi-automated equipment. Jim Carden, manager of mechanical CIM for Tektronix, claims that this setup has resulted in significant production increases and has shortened the design cycle at his company.

Another electronics company using this type of "remote-controlled CIM" is Racal-Milgo Inc. in its personal-computer-board assembly operation. Design data from an engineering data base in Sunrise, Fla., is sent over a microwave link to a host computer in Miami to control several interlinked operations: two pc-board assembly lines (one a highly automated flexible-board line), in-circuit test, and systems test. The company uses GenRad's Test and Repair Analysis Control System to gather process data in the assembly areas, correlate it with data from the test stations, and provide management with the real-time information needed to control quality and productivity.

This system has increased board output by 50% and reduced the number of employees needed for fault detection, the company says. In addition, the cost of direct labor was reduced to less than 5% of overall product cost. At the same time, defects in workmanship dropped by more than 80%.

Along with the application of CIM, another development that's gathering steam is the appearance of expert systems in the manufacturing chain. Tektronix, which has a separate product group for developing artificial intelligence products, is starting to integrate this capability into manufacturing.

CAD/CAM. At Tektronix, CAD data is converted to a machine insertion program for loading a pc board with packaged ICs.

One of the company's first efforts is an expert system, now under development, for intelligent scheduling and machine mode operation. This unit will take information from a Manufacturing Resource Planning source and decide on what resources are available. MRP alone is an open-loop system and cannot do this.

In another AI effort along these lines, Lockheed-Georgia Co. in Marietta, Ga. has created an expert system called Assembly Genplan tthat incorporates the equivalent of 300 years of assembly planning, all garnered from human planners. Genplan's creators picked the brains of experienced assembly planners, who were asked the best ways to accomplish various airplane assemblies. This expertise was fed into a sophisticated computer-knowledge data base.

EXPERT SYSTEMS IN THE SHOP

Meanwhile, other expert systems have shown up on the shop floor. For example, at Texas Instruments Inc.'s Trinity Mills facility in Carrollton, Texas, an automated manufacturing system machines, deburrs, and cleans raw aluminum casings without human intervention. A diagnostic expert system based on the TI Personal Consultant helps operators identify and solve problems without having a communications expert on hand at all times.

In the near future, expert systems are likely to be used in situations where knowledge is perishable, scarce, and difficult to apply—namely, planning, manufacturing, engineering, test, and maintenance. For example, the multimillion-dollar testers for very large-scale integration-circuits now starting to appear will certainly need a maintenance expert to minimize their downtime. That expert may well be an AI machine.

While the glamorous expert system is poised to make an impact on manufacturing, the flexible manufacturing system is already having an effect on IC manufacturing. Both National Semiconductor and Texas Instruments, for example, are engineering flexible lines for IC assembly. National's new Odyssey assembly line should go on-stream in mid-1987, and TI is redesigning and updating its Flexible Assembly Module. When they are completed, both facilities will be able to turn out many types of IC packages on the same, reconfigurable line.

Odyssey will use either wire bonding or tape-automated bonding to produce a variety of package types, such as dual-in-line packages, chip carriers, or small-outline packges. The redesigned TI Flexible Assembly Module—which now produces only DIPs—will turn out SOICs by the end of 1986 and quad flatpacks by 1987.

CONSUMER

Technological advances continue to spur new offerings in VCRs and camcorders, while developmental work continues on higher-definition television receivers

by Samuel Weber

Within the next two years, digital technology will begin to dominate audio and video designs, beguiling consumers with such enhanced products as video cassette recorders that feature still and slow playback, picture search, and picture-within-a-picture. The already sensational sound quality of compact disks will improve as manufacturers strive to reach the theoretical limits of the medium by using higher-density circuits in compact-disk players. And high-definition television with high-fidelity stereo sound will move closer to the consumer's "most wanted" list.

Many Japanese manufacturers were hoping to introduce digital audio tape machines this year, but two problems cropped up that appear to have stalled progress. One is fear that the product will cut into sales of CD audio gear. The other is that nobody has come up with a foolproof method to foil copying. Pirating is a much more severe problem with digital than with analog tape, because each generation of copies would theoretically be indistinguishable from the original in quality.

Field memories are finally appearing in VCRs that make possible a range of unconventional playback modes. In some of them, the sound continues while the individual fields flash on the screen at a rate chosen by the viewer. A unit from Hitachi Ltd. permits control of a number of brightness levels. With another mode, picture-in-picture, viewers can watch video on the full screen and TV from the VCR tuner on an inset, or vice versa. Besides Hitachi, VCRs with some of these souped-up features are also available from Victor Company of Japan (JVC), Toshiba, and Sharp; Matsushita, Mitsubishi, and Sanyo are ready to introduce products.

All the VCR offerings use field memories with a digital resolution of only six bits, enough so that the reproduced picture quality is better than that of stills reproduced directly from tape. No critical mechanical adjustments or extra heads are needed for still playback.

Because of limitations in memory capacity, all manufacturers appear to be sampling at 10.7 MHz. This is adequate for picture storage only, but for digital processing in both VCRs and TVs the sampling rate of choice will probably end up

HIGH FIDELITY. Audio waveguide technology developed by Amar Bose brings better sound to a Zenith digital TV.

TURNING THEM OUT. A West German VCR plant looks busy, but demand is slacking in Germany. Digital technology may revive it.

at four times the 3.58-MHz color-subcarrier frequency, because it simplifies circuit design.

Toshiba uses standard dynamic random-access computer-memory products—both 64-K-by-4-bit and 64-K-by-1-bit chips. Storage of one field requires a total of 64-K by 18 bits, or four 64-K-by-4 chips plus two 64-K-by-1 chips. JVC uses a special field-memory chip developed jointly with NEC Corp. about three years ago.

Hitachi goes all-out in one VCR model and includes two types of memories—a field memory and a smaller memory for picture-in-a-picture. For the former, it uses six NEC field-memory chips for a 64-level gray scale and a seventh for synchronization. For the latter, it uses two NEC 64-K-by-4-bit dual-port RAMs.

This is the year that 8-mm camcorders—first announced in January 1985—should have blasted off. They didn't, though, because JVC developed VHS-C units that at 1.3 kg are lighter and smaller than the 8-mm products, which typically weigh in at around 2.3 kg. The compact VHS cassettes provide only one hour of playing time compared with two or more hours for 8-mm units, but for most consumers that's enough.

The 8-mm camcorders won't supplant the ½-in. VHS-C format, says John Osterhout, planning director for consumer electronics products at Eastman Kodak Co., which is pursuing the 8-mm market. But he expects 8 mm to be the growth product over the next 10 years, in large part because 8-mm software will cost less. Among the enhancements is a multiplexed signal to extend luminance bandwidth from 4.2 to 6.0 MHz. These products could reach the market by 1989.

Aside from VCRs and camcorders, much work is under way in Japan on improving TV picture quality, which is coming in three stages—improved-definition TV, extended-definition TV, and high-definition TV. Improved-definition TV consists of improvements in standard NTSC TV, among them noninterlaced scan implemented with line memories, which both Hitachi and Sony are already offering. Toshiba has just joined the race.

Extended-definition TV refers to a Japanese Ministry of Posts and Telecommunications project to develop an enhanced broadcast signal with improved horizontal resolution. High-definition TV refers to the 1,125-line TV system developed by NHK. Exactly when a consumer version of either will be available is unclear.

In the U. S., at least one TV maker is concentrating on better sound quality. Zenith Electronics Corp., in Glenview, Ill., recently introduced a 27-in. digital TV set equipped with a high-fidelity sound system designed by Bose Corp. chairman Amar G. Bose. Bruce Huber, Zenith's vice president of marketing, says additional Zenith models incorporating Bose audio technology will appear in the next year. They won't necessarily rely on the same kind of low-frequency waveguide technology employed in the audio section of the first sets [*Electronics*, Aug. 21, 1986, p. 40].

As for digital TV per se, Huber notes that it "certainly hasn't set the world on fire." But he foresees better digital penetration as the digital technology moves down from the high end to manufacturers' mainstream receiver lines. Zenith has six digital sets on the market, but so far has chosen not to offer features like the picture-within-a-picture. Instead, the company is concentrating on other enhancements, including its World System Teletext decoder, the first TV-teletext system in the U. S.

In Europe, TV producers are also turning to digital technology. The ITT subsidiary Intermetall GmbH—which pioneered digital-TV circuits in 1983—is offering chip sets for video and audio processing that help streamline set production. Philips International NV in the Netherlands has introduced a digital solution that builds upon and supplements analog processing to improve picture quality. Central to the Philips solution is a 320-kb charge-coupled-device memory, a store for video signals that cuts down flicker, helps produce still pictures, and provides a picture-in-a-picture facility. □

PROBING THE NEWS

IS THE ATE MARKET HEADED FOR A SHAKEOUT?

OBSERVERS CITE IC SLUMP, BUT MOST DON'T SEE FALLOUT FOR 5 YEARS

by Larry Waller

To some industry experts, signs now point strongly to a major shakeout of suppliers coming in the high-performance end of the automatic test equipment market. The main reason, they say, is that the industry's largest customers, those makers of the latest very-large-scale integrated chips, don't have the money to spend on new systems because of the protracted slump in the semiconductor business. Top-of-the-line ATE systems carry high prices—$1.5 million and up for VLSI logic testers and nearly half that for megabit memory testers.

Also beginning to hurt these ATE makers, experts add, are soaring research and development costs and overcrowded ranks. At last count, nine mainstream companies offered ATE gear, and several more were in the wings.

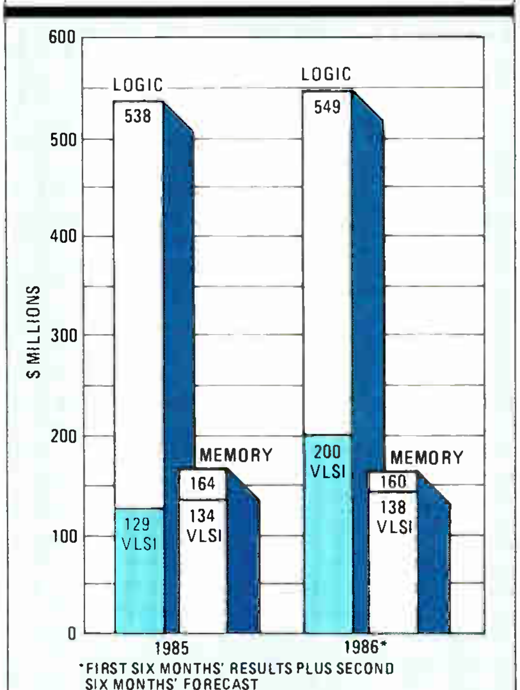
A shakeout is in fact already under way, says industry watcher Stephen J. Balog, financial analyst at New York's Prudential-Bache Securities Inc. "There are too many players, which means too many testers chasing too few testing-floor slots." Because the costs of developing the new generation of VLSI testers run so high, upwards of $5 million per system, the industry spends a very high 20% of sales on R&D.

Balog cites several companies as evidence that the shakeout has begun. Cybernetics Technology Corp., makers of an ambitious 256-pin Model V200, which used a supercomputer architecture to achieve a 100-MHz data rate, has gone out of business. Accutest Corp., which was offering the Model 7950, a 50-MHz unit, has closed up shop. And Hewlett-Packard Co. has withdrawn from the memory test business, Balog adds. In his view, the ATE market dropouts not only will continue—the pace will accelerate until the number of competitors declines sufficiently to balance with demand.

But to most experts, whether all this adds up to a shakeout is open to question. Some market watchers maintain that the chances for a substantial realignment of suppliers any time soon are slim—that nothing much will happen for at least five years. Even executives among ATE companies, who would like nothing better than a little less competition in a business where each sale is hotly contested, don't expect the lineup to change much in the short run.

The distinction they draw is between the costly top-of-the-line VLSI machines, those with 200 testing pins and data rates above 40 MHz, and the rest of the field. Sales of big testers will grow, even though the lower levels of ATE products are "a disaster," says market analyst G. Dan Hutcheson of VLSI Research Inc. in San Jose, Calif. The improvements in big systems work through an entire line, softening the impact of R&D costs. "The key thing to remember is that VLSI testers are at the forefront of technology. The [ATE] companies have to be in, or they're doomed to be second-tier suppliers."

VLSI LOGIC TESTER SALES JUMP



*FIRST SIX MONTHS' RESULTS PLUS SECOND SIX MONTHS' FORECAST

SOURCE: VLSI RESEARCH INC.

Hutcheson has another reason for being more optimistic. This is the first full year on the market, he notes, for the latest logic testers. The chip makers must have the powerful new test gear to stay competitive. That is why the VLSI logic testing segment in particular "is actually doing very well, up about 83% in 1986" (see graph below). Also, he adds, "Every recession, people talk about a massive exodus, and it doesn't happen that way. This [testing] is a slow-moving business."

But other industry experts, who like Hutcheson see no shakeout happening now, acknowledge that the roster of ATE suppliers has to shorten, perhaps to as few as four companies worldwide. Unanimous choices for the survivor list are two Japanese outfits: Advantest Corp. and Ando Electric Industrial Corp. Not only have they grabbed leadership roles in their important home market, but their ties to giant industrial companies—Fujitsu Ltd. has a 21% equity in Advantest, and Ando is 51% owned by NEC Corp.—lend them the financial stability needed to go the distance. And besides a dominant position at home, they are positioning themselves to get a larger part of the U. S. tester business (See "Japanese ATE makers still wait for the 1-Mb RAM boom," p. 112).

The third name on the list, market watchers agree, will be Teradyne Inc. of Boston, on the strength of new product development and sales gains over the past few years. This year, Teradyne's Semiconductor Test Division in Woodland Hills, Calif., introduced the industry's first megabit memory tester, the J937, and made its first U. S. delivery of the product late last month. Also, it is mounting a challenge to Advantest and Ando on their own turf with the J937 through an organization expanded to 150 people from 60 two years ago. [*Electronics*,

HOW THEY RANK IN TESTER SALES WORLDWIDE		
Logic	VLSI logic	Memory
1. Advantest	1. Ando Electric	1. Advantest
2. Ando Electric	2. LTX/Trillium	2. Teradyne
3. Schlumberger/Sentry	3. GenRad	3. Schlumberger/Sentry
4. GenRad*	4. Megatest	4. Megatest
Teradyne*	5. Teradyne	5. Ando Electric

*In a virtual tie for fourth

SOURCE VLSI RESEARCH INC.

March 31, 1986, p. 52]. The increased competition throughout the tester business, says Teradyne's James A. Prestridge, who heads the Component Test Group, will end up "gradually squeezing out the least efficient producers, not [causing] a massive shakeout."

UP FOR GRABS. After those three companies, says Balog, "the other slots are up for grabs." His contenders, all of whom are vigorously marketing new VLSI testers, include the onetime king of the business, Schlumberger Ltd.'s Sentry Division; GenRad Inc.'s Semiconductor Test Division; and Trillium Corp., a subsidiary of LTX Corp. Also, Tektronix Inc. recently dealt itself into the game with its Model LT-1000, a 256-pin, 50-MHz production tester.

Other players are Megatest Corp. and Semiconductor Test Solutions, both heavily backed by venture capital. Insiders place the total investment for both near $60 million, with more available if they need it.

Trillium has taken on some luster with its $1.5 million ArrayMaster, a 50-MHz unit for testing CMOS gate arrays. The company has racked up $22 million in revenue since introducing the machine in August 1985, including a contract with Intel Corp. announced last month. This surge causes Balog to say, "LTX/Trillium is now in the club," with a good shot for long-term survival. His only caveat: does the smallish company have the financial staying power to flourish in a business that eats up capital?

Such financial depth is the key ingredient, given the right product, says Sentry's Fred Laccabue, whose firm has been the subject of many dropout rumors. He says Sentry's newest entry, the Series 90 megabit memory tester, demonstrates the commitment of parent Schlumberger, which also owns Fairchild Semiconductor Corp. "The $10 million investment speaks more clearly than any promises," he says. Sentry also has made 14 sales of its 50-MHz Model 50 VLSI tester, which carries a price tag of $2 million to $3 million, since May 1985, including several in the Far East.

For GenRad's part, its new Model GR180, with an 80-MHz data rate, is the only tester aimed specifically at devices in the Pentagon's Very High Speed Integrated Circuit program, a potentially lucrative segment. The first order for a GR180—which goes for $2 million to $4 million—has come in, and GenRad expects more, says Gene Roth, marketing manager at the test division. The firm claims an installed base of some 100 other VLSI systems among 50 different customers, which Roth says "positions us well."

San Jose-based Megatest also appears well positioned. It says that sales of its 40 MHz MegaOne tester, first delivered in 1985, are doing well at up to $2.5 million apiece, with 25 due to be installed by the end of the year.

Balog hears all the upbeat talk, but he's not convinced. "Some of those guys are just whistling past the graveyard. A couple more disastrous quarters and we'll see it." □

JAPANESE ATE MAKERS STILL WAIT FOR THE 1-Mb RAM BOOM

As recently as three months ago, a Tokyo analyst wrote that VLSI testers were "the one bright spot in the industry" because of the demand for 1-Mb random-access memories that was expected by fall. Now, say the analysts, there are no strong signs of the long-awaited recovery in any commodity product market, and the two leading Japanese tester makers have revised their estimates sharply downward even as they look to overseas markets.

Ando Electric Industrial Corp.'s operating profit margin will be squeezed this year to 8.5%, half the figure of last year, and Advantest Corp. is looking at zero growth.

A major weak spot is the slower-than-expected changeover from 256-K to 1-Mb memory in Japan, although development work on the chips is moving along. The changeover is being slowed further by the recent U. S.-Japan semiconductor marketing agreement. The pact has given Japan's chipmakers a sudden chance for windfall profits on 256-K products under the so-called "foreign market values" established by the Department of Commerce. Toshiba Corp., which boldly predicted it would be making 1 million 1-Mb chips monthly by now, is producing barely half that amount. Other major makers, such as Hitachi, Fujitsu, and NEC, are at the 200,000-to-400,000 level.

Meanwhile, the Japanese have been selling overseas, especially in the U. S. Advantest, which effectively targeted Fairchild customers in the U. S. at a time when the market leader was slipping, built sales there to about $30.4 million last year, almost double the year before. But this year, growth will be virtually flat.

Ando, which has emphasized logic and linear testers in building its sales 50% over the past two years, has had a strategy of following NEC to its overseas production sites. Its U. S. subsidiary, Ando Corp., assembles, sells and services its IC tester systems. The company also has a telecommunications measuring equipment plant in Maryland. Total U. S. sales were about $20 million in fiscal 1986, and there are plans to produce both test and measurement systems in America by the late 1980s.

But the Japanese, say industry insiders, have a weak spot: less-than-impressive software to go with their impressive hardware. Advantest, which as recently as three years ago subcontracted much of its software development, has established one U. S. subsidiary (Advansoft Research Corp., Santa Clara, Calif.) and three in Japan. Ando also has a software subsidiary in California, but both companies have had difficulty in recruiting good engineers.

Meanwhile, the slump is wreaking havoc with plans for new systems. "We thought at first the recession would help us, because our J937 series is the first megabit memory test system," says Richard Dyck, president of Teradyne KK, the Boston-based maker's Japanese subsidiary. Not only have Japanese customers' appetites dulled for $350,000 systems, but rivals Advantest and Ando have gained time to develop their own product lines. Teradyne's original 18-month market lead is rapidly disappearing.

Fairchild, which dominated the market a decade ago and then was overrun by the Japanese, has been counterattacking since its takeover by Schlumberger Corp. two years ago. Alex Beavers, vice president and general manager of Schlumberger Computer-Aided Systems Asia (Tokyo) says the company has introduced its own megabit memory tester, the Series 90. Beavers says the new product will be introduced to Japan early next year, at the same time that the Teradyne and Japanese models are due for entry. *–Michael Berger*

JAPAN FINALLY GETS AN EASY WAY TO TALK VIA COMPUTERS

ONE RESULT COULD BE A TERMINAL TO REPLACE THE PHONE

by Charles L. Cohen

In the U. S., the communications modem is a common accessory among microcomputer owners. But in Japan, that is not the case: until recently, Nippon Telegraph & Telephone Corp. did not permit use of its lines. That is why a government-backed development called JUST-PC, a communications controller that includes a modem and promises simple, error-free communications, is so significant.

JUST-PC, an acronym for Japanese Unified Standards for Telecommunications for Personal Computers, operates according to a series of protocols that conform to the seven-layer Open Systems Interconnection model of the International Standards Organization. Proposed applications range from a simplified visual-information terminal that could replace the telephone, to services involving a mainframe host. A wide selection of communications applications among conventional personal computers will occupy the middle range.

The adapter that implements JUST-PC—including a built-in communications controller with attendant software and a modem—provides full-duplex communications between different types of personal computers or between them and a host. The computers can even talk to other types of equipment, such as distant facsimile.

The most popular application for JUST-PC among the preliminary installations now in operation is access to an experimental free mailbox and bulletin-board service operated by NTT PC Communications, a subsidiary of Nippon Telegraph & Telephone Corp. It is scheduled to convert those into commercial services next month. Other large-scale value-added networks planning to start service soon are expected to offer their own JUST-PC services. And several companies are already vying for a share of the adapter market.

JUST-PC can also access NTT's Captain videotex system, and all it will take is a change in the data rate at the network center for JUST-PC to interface with Japan's packet-switching network and with G-4 digital facsimile.

Although most experts extol the ability of JUST-PC to provide error-free connection, at least one former project leader sees its importance in its simplicity. "It can be used by anyone, because the adapter completely handles communications protocols," says Shuichi Shimokoba, manager of customer equipment at NTT. Ordinarily, some expertise is needed for successful personal-computer communications, says Shimokoba, who spent three years on loan to the Ministry of Posts and Telecommunications during the project.

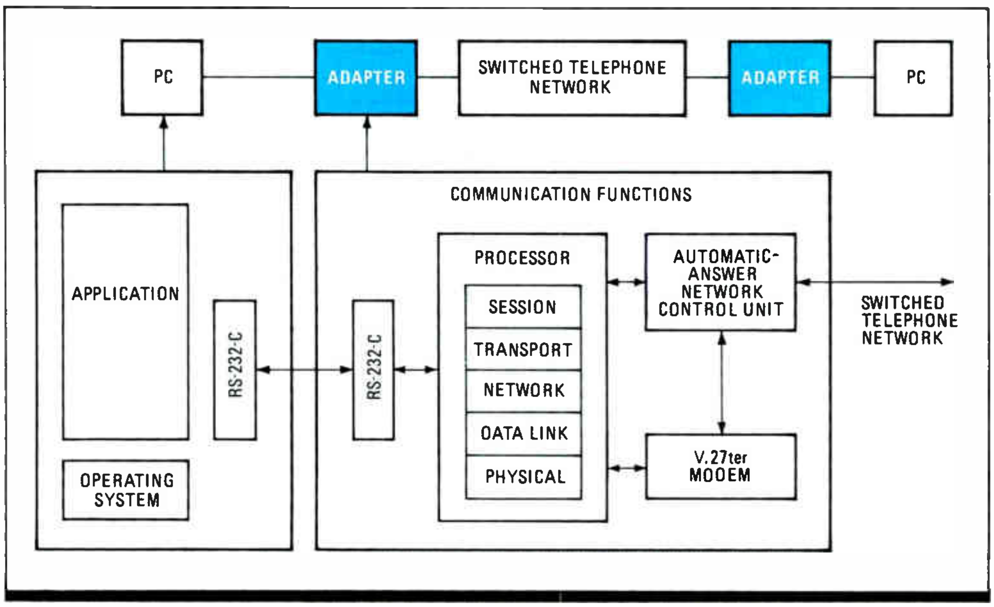
CONSUMER SALES. Moreover, he says, "the standard automatic-answer facility lends JUST-PC an important characteristic shared with the telephone, TV, and facsimile, today's most widely used communications terminals. How many people would have their own telephone or facsimile if they couldn't receive calls or transmissions? That feature will generate consumer sales, driving down the price and providing less-expensive units that are more convenient and reliable than the usual run of office or professional systems."

Also, the system avoids draining the computer's resources—unlike many communications programs involving complex protocols, which use much of the power of the computer, leaving very little capacity for applications. Simpler communications programs tend to prevent applications from accessing the full power of the computer, leaving its resources wasted.

Shimokoba looks beyond the mailbox and bulletin-board services to the day when the price of JUST-PC can be brought down to what today's 1,200-b/s modems cost, making its full potential available to users without much regard for the cost of the equipment. He says that above 2,400 b/s, synchronous rather than asynchronous modems will be needed, so standard protocols will be needed in any case. JUST-PC can freeze the protocol and switch to voice communications, a capability not provided in other communications schemes, he says.

Right now, software is the key. "The growth of JUST-PC depends on the availability of software" that his and other software companies are developing, says Kenichi Takahashi, manager of the Systems Sales and Marketing Department at Ascii Corp. "It will be especially strong on transmission of natural graphics, including 256-color graphics or digitized picture screens."

One of the potential uses of JUST-PC,



SIMPLE. Computer, seeing JUST-PC adapter as a communication function, sends through RS-232-C port.

as a successor to the telephone, is being demonstrated by a Tokyo startup company, KK Meta-communications, in the form of a nonfunctional mockup called a visual information terminal. The mockup looks like a streamlined 12-in. computer monitor with a recess on top for a telephone handset. The initial price will be about $2,700 to $3,300, says Yoh Tanaka, a visiting professor of industrial design at the Tokyo National University of Arts and Music who has started the company especially for the project.

These terminals will provide three capabilities not available in current communications systems, says Tanaka. The first is called precommunication, in which the caller is identified on the screen, enabling the person getting the call to select the most convenient method of handling it. The second feature is networking, similar to the infrequently used telephone conference call. And the third is radial communication, which sends the same message simultaneously to a number of recipients.

VERSATILE INTERFACE. The visual information terminal will feature 4 megabytes of memory and a command menu. Simple data input is provided by touch-screen facilities; users who want to enter text or substantial amounts of numerical data will be able to connect the terminal to the increasingly popular Japanese-language personal word processors. They will also be able to attach a handwriting input unit or a scanner.

Some applications envisioned by Tanaka resemble those for videotex or similar services. As an example, he cites ordering from a menu provided by a shop, making travel reservations, using remote control of a video cassette recorder to record a TV program, or other so-called home automation tasks. But the visual information terminal differs from many services that have preceded it, such as Knight-Ridder's videotex operation in the U. S., because the real task for the terminal's vendors is to develop new kinds of applications for the technology, rather than to find ways it can be used for applications that customers already know they want.

Applications and display design are being developed by Tanaka. KK Meta-communications will develop applications, and actual software will be developed by another small firm, KK MP Technology, established by Yoshimoto Masuo. Initially, the terminals will be made by a limited number of manufacturers and field-tested in a closed market. An emulator using NEC's popular PC-9801 microcomputer is expected this month.

Tanaka says that the visual terminal is a case where designers must create a need, not serve one. "Technology has advanced to the point where obvious needs have been fulfilled and a new theory is needed to know what to make, and for what purpose," he says.

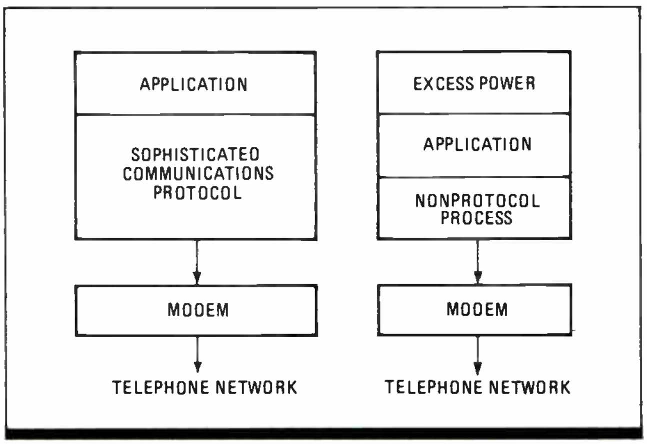
For JUST-PC, a half-duplex modem provides what appears to the user to be full-duplex service. The system is designed around the industry-standard V.27ter modem. Operating at 4,800 b/s with fallback to 2,400 b/s, this modem is widely used in industry-standard G-3 facsimile equipment to provide transmission over analog lines. It was selected because it is fast and a proven design, and it is inexpensive because it is so widely used in facsimile.

JUST-PC uses an adapter that fully implements all functions of the five lower layers of the OSI standard, including the modem. Only the presentation and application layers must be implemented by the application program. Then a simple three-wire connection to the adapter and minimal supporting circuitry, including an RS-232-C driver, adapts a personal computer to JUST-PC. The adapter operates in full-duplex mode with error checking, enabling it to handle text, binary data, or bit-mapped data.

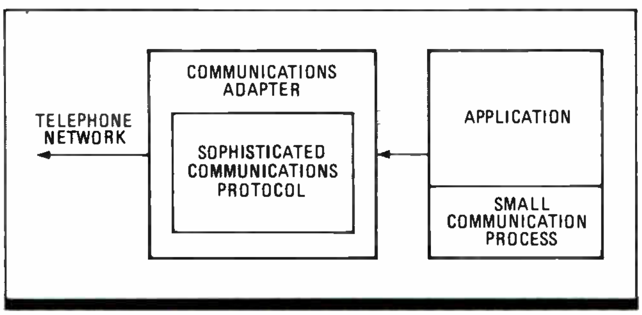
Like other error-checking schemes, the one in JUST-PC slows the data rate. Even that penalty is less than that encountered in most personal-computer communications schemes—data can be transferred one-way at nearly 4,000 b/s. And although a number of error-checking schemes are used in the U. S. and elsewhere for modem communications, none is universally available, says Toshiyuki Takei, a staff engineer at the Ministry of Posts and Telecommunications. On the other hand, system error-checking is standard in Japan and is available for all types of data transfer.

ATTRACTIVE MARKET. The market for JUST-PC is attracting a lot of attention, chiefly because getting into it shouldn't cost too much. Modem chips or boards are available from a number of manufacturers, and the remainder of the adapter uses standard parts, including a Zilog Z80 microprocessor and peripherals. Modem chip sets are available from Toshiba Corp and Nippon Gakki; modem boards are available from Oki, Matsushita Graphic Communication Systems, and Rockwell International. NEC makes chips and boards but doesn't sell them as components.

JUST-PC also requires only a simple software interface to the adapter—programmers do not need expertise in the intricacies of communications protocols. Applications that would have taken six months to write can now be done in two weeks, because they are similar to available applications that do not involve communications.



NOW . . . High-end communications tools drain resources from large applications, left; but low-end tools can't run big applications, right.



. . . AND WITH JUST-PC. Sophisticated communications functions are provided by the adapter without imposing a large load on the system.

The system most likely will create a lively market in adapters. The biggest vendor so far is NTT PC Communications, 10% of which is owned by Logic Systems International Inc., a Japanese manufacturer of personal computers and communications equipment. Logic Systems designed NTT PC's adapters, which are made by a contract assembler.

But Logic Systems is not alone. Fujitsu, Hitachi, Iwatsu, NEC Corp., and Oki Electric Industry are also making JUST-PC gear. And Mitsubishi Electric appears ready to join the crowd.

List prices range from $800 to $950, but should drop as sales increase. Prices would probably drop still further if the International Telegraph and Telephone Consultative Committee's SG-8, which is considering JUST-PC, adopts it as a worldwide standard. However, government engineer Takei says that might not happen, because other nations have vested interests in videotex and other services. □

The evidence is in, and it's incontrovertible. When it comes to light, Anritsu runs second to the sun.

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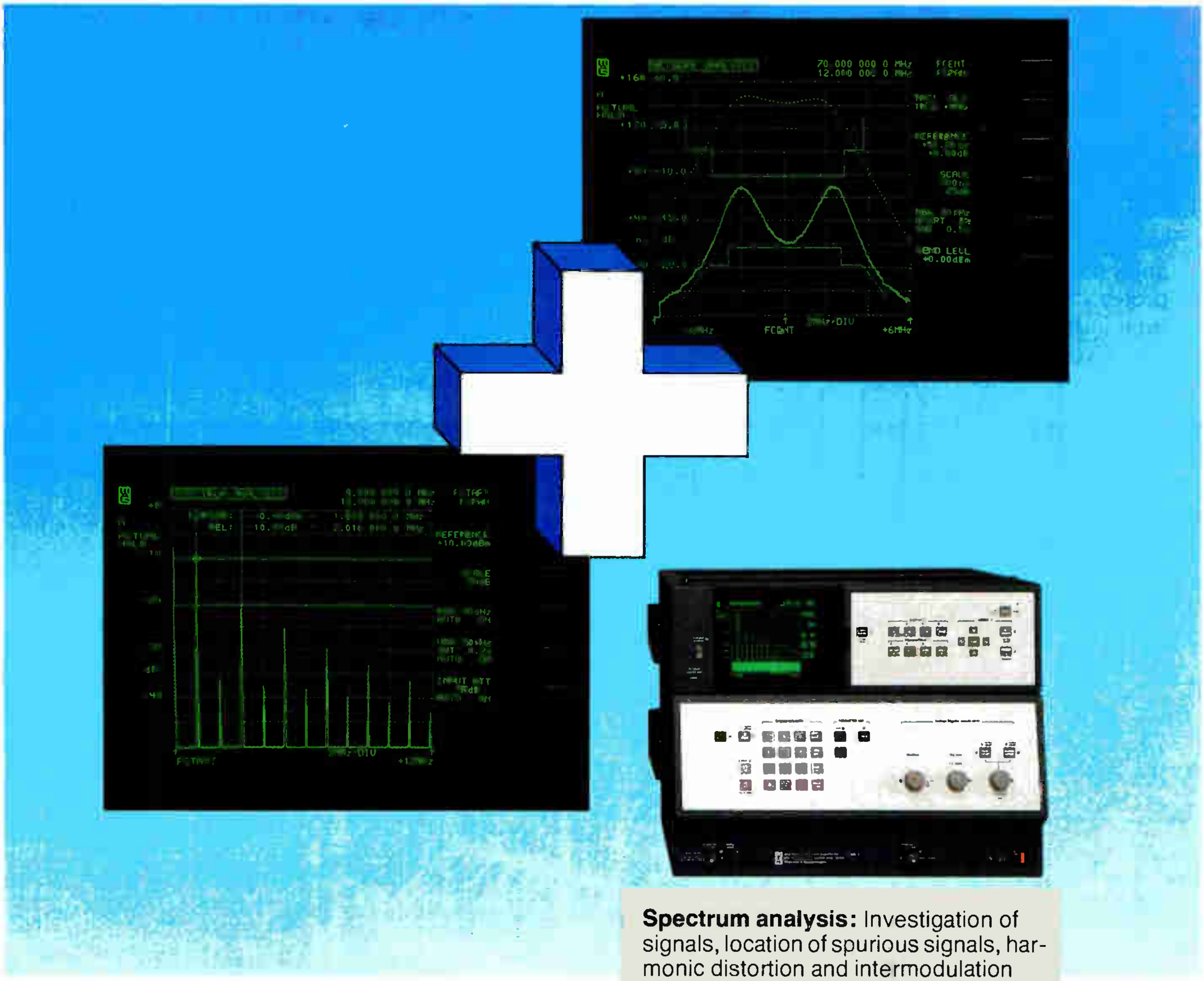

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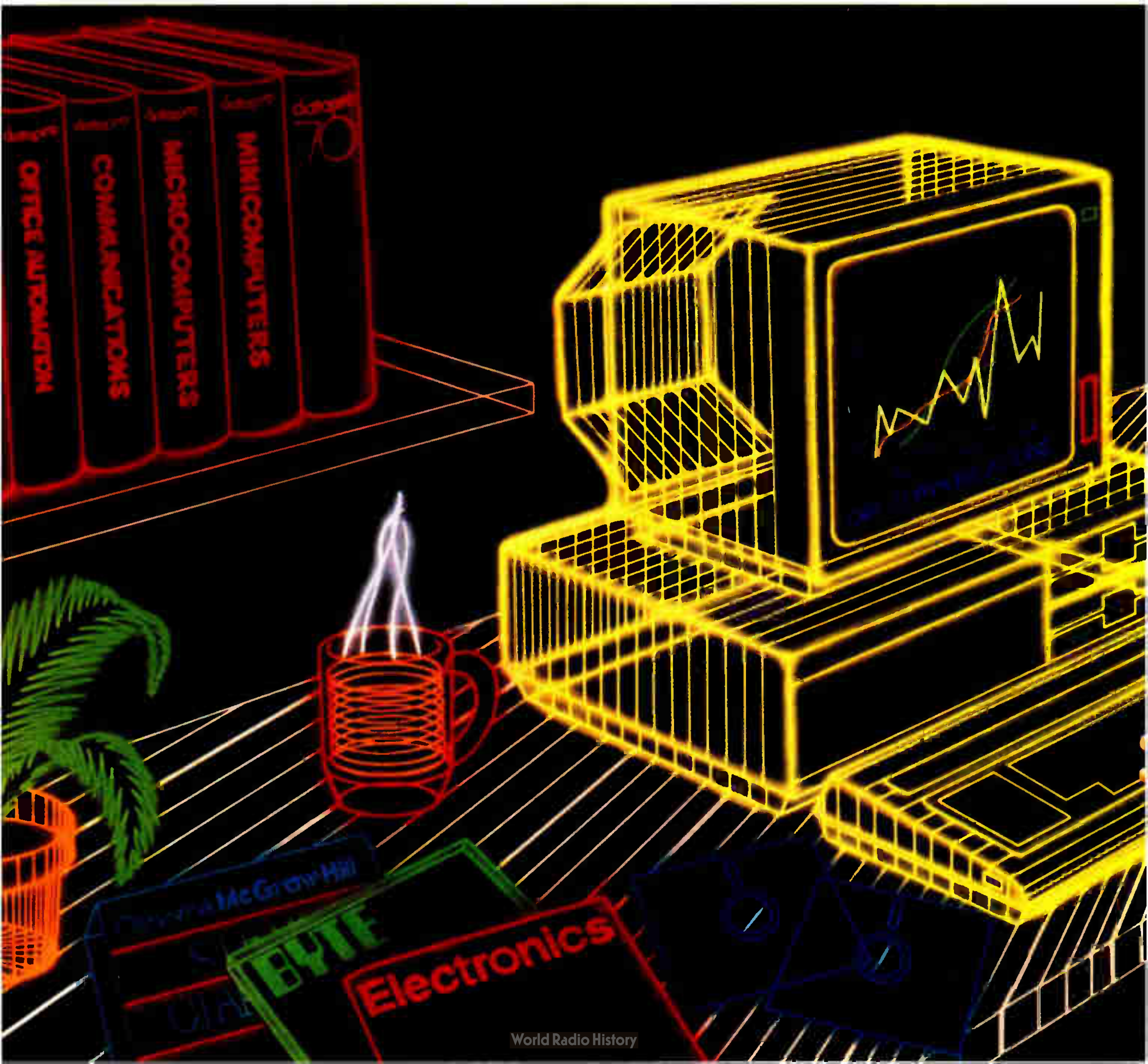

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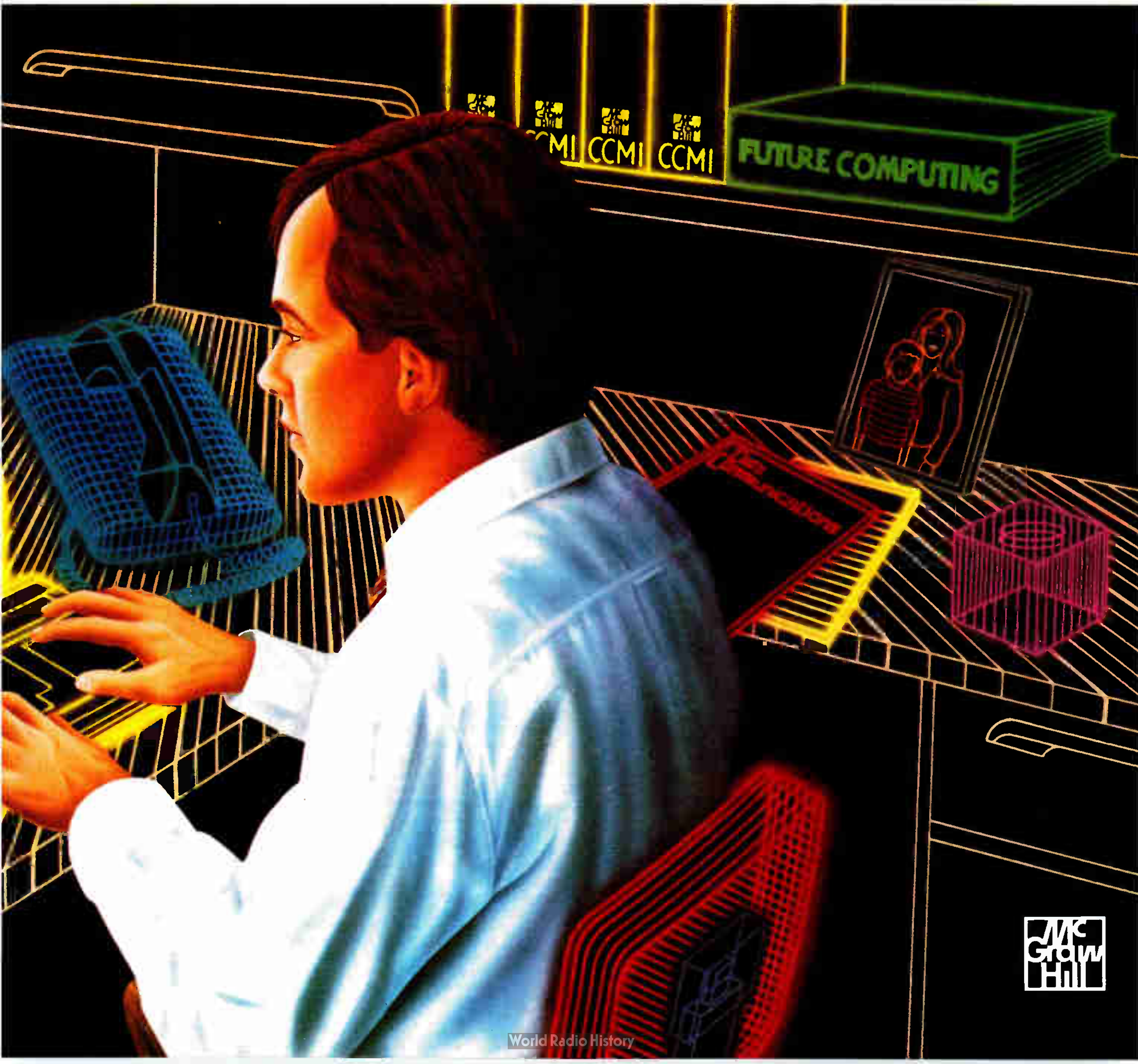

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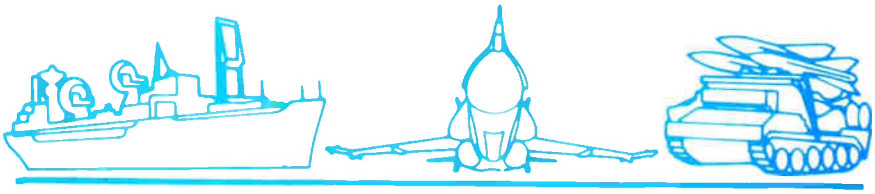


MILITARY ELECTRONICS

SPECIAL ADVERTISING SECTION

Targets of opportunity abound for anyone willing to take a shot

The Defense Department's annual budget for electronics continues to inch upward as the military puts more emphasis on high technology and improving weapon systems. Much growth will come from the opening of the tactical computer market, new hardware and software systems, ongoing high-ticket programs such as the Strategic Defense Initiative (better known as Star Wars), and new Air Force research and development proposals. But there are also plenty of opportunities for companies to participate in somewhat smaller, if only slightly less ambitious, programs.

The Electronics Industries Association's Government Division believes that over the next 10 years the electronic content of the DOD's budget will grow just over 3%, despite a projected 3% decline in the overall defense budget. The division is scheduled to release its updated projection of the military electronics market later this month.

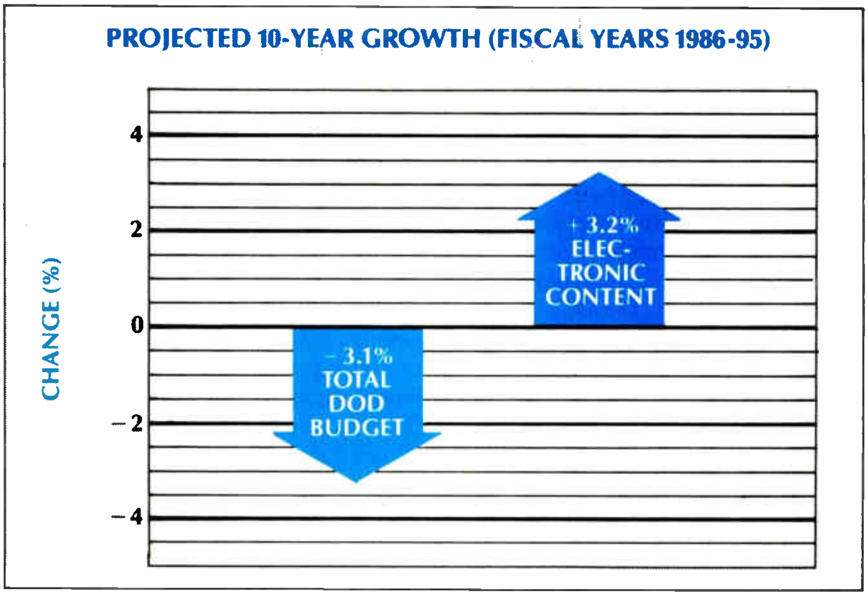
For some manufacturers, the military is an increasingly important customer. Texas Instruments Inc., Dallas, reported recently that its growing military electronics sales helped offset a poor showing in some of its commercial markets. A number of companies, mainly hardware and software vendors, are entering the military market or expanding their presence in expectation of major buys by defense agencies over the next few years. For example, General Instruments Corp.'s Microelectronics Division is revamping its marketing group in Chandler, Ariz., in an effort to win more military business.

Further evidence of how important defense electronics is becoming can be found in recent merger and acquisition activity. Lockheed Corp. in Sunnyvale, Calif., primarily a military aircraft producer, recently acquired a major stake in Sanders Associates Inc., a Nashua, N. H., defense electronics company, in what industry observers view as an attempt by Lockheed to improve its position in upcoming advanced combat-fighter contract bids for the Air Force and Navy. Loral Corp., Yonkers, N. Y., which lost out in an earlier attempt to acquire Sanders, says it will continue to look for "complete-system" defense contractors.

Other major military aircraft manufacturers, including Boeing, McDonnell Douglas, and Rockwell International, also have publicly expressed an interest in defense electronics acquisitions.

Some observers, however, are expressing less faith in the military market. In a report issued last month, Henderson Ventures, a Los Altos, Calif., market researcher, called military electronics one of the few industry bright spots during 1986. But it expects the market's growth rate to decelerate from a 9.3% rate this year to 3.2% in 1987. Conversely, Henderson says the rate of expansion for commercial electronics will accelerate from 2.9% in 1986 to a respectable 13.4% next year.

At the moment, notes Henderson, the military electronics market remains deceptively vibrant. Next year, however, the research organization says that Gramm-Rudman-inspired



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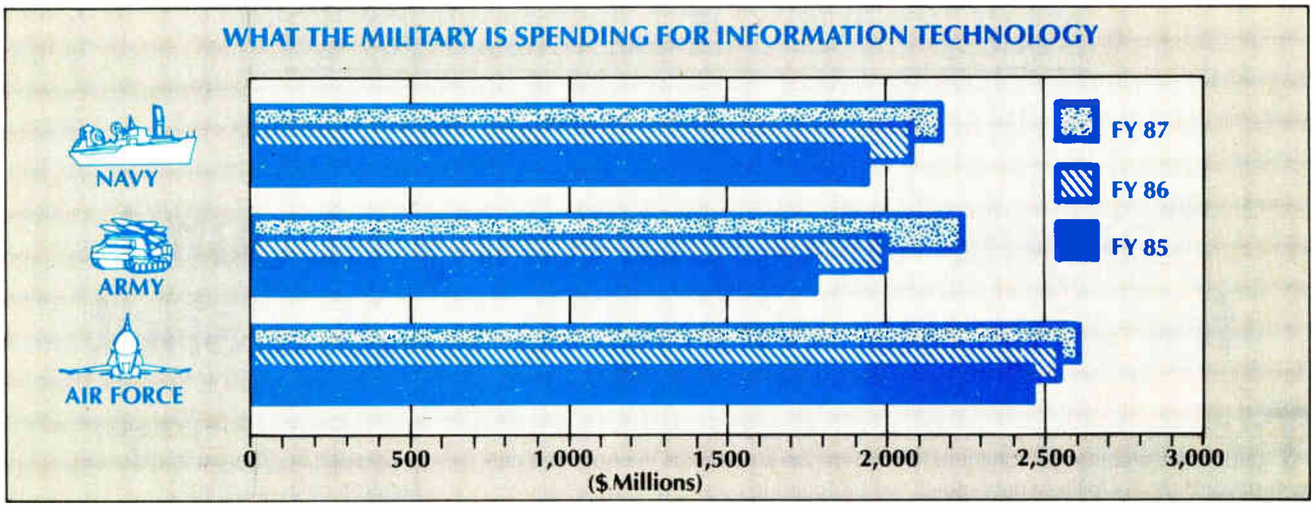

Source: DOD

budget-balancing legislation will force a sharp slowdown.

Its analysis of the military electronics market calls for an increase from this year's $50.16 million to $51.76 million in 1987. Pentagon spending on electronics will climb to $54.78 million in 1988, according to Henderson. In real terms, however, calendar year outlays for defense spending will decline by 2.6% during 1987, after a 3.3% increase in 1986.

At the Columbus Division of Battelle Memorial Institute, a research and consulting organization in Ohio, M. R. Vanderlind, director of electronic and defense systems, says that "DOD budgets will be very tight. The impact of Gramm-Rudman [budget-balancing legislation] will come into play—indirectly, but it will have a real impact. And more attention will be given to deficit spending."

Another long-time analyst, Bob Dornan, vice president of Federal Sources Inc., a Vienna, Va., firm that advises industry companies seeking government contracts, sees a healthy rise in expenditures in many areas, including computers and telecommunications. Nonetheless, he believes Gramm-Rudman will temper that to some degree. "Some programs were never really very popular, and Gramm-Rudman will be used as an excuse to kill them."

Embedded computers, in particular, will be a major target of opportunity because virtually every defense system is dependent on computers and software. "We have over 185,000 computers in the field now, not including microcomputers, and we expect that number to double in three years," Donald A. Hicks, Undersecretary of Defense for Research and Engineering, told the recent American Defense Preparedness Association Conference on Military Computers and Software.

Focus on software

With software accounting for about 80% of a computer system's cost, the DOD is giving it a lot more attention. "There are more than 120 defense systems under development that are critically dependent on software," Hicks noted. "We estimate the software requirement for these systems at about 150 million new lines of code." The DOD, which currently spends about $10 billion a year on embedded software, expects to be spending more than $30 billion a year on software by 1990—over 10% of the defense budget.

Underlying the DOD's projection are recent studies by the Institute of Defense Analysis and the Air Force. The institute concluded that at least 70% of all DOD weapon systems in the planning or procurement cycle today depend on software technology. In fact, many new systems cannot operate at all without software. Moreover, the study found that field studies of several major systems, new and old, confirmed that the state of the art in military computers lags by up to 15 years.

The Air Force's report shows greater demand for software development in the U. S. than potential suppliers can fill. It also says that DOD mission-critical computer software has more requirements than qualified, or qualifiable, software development contractors can handle.

According to Hicks, the DOD will need a new generation of computers for use in mission-critical systems by early 1992. "Our preferred approach for the next generation is to work with industry to develop suitable common interfaces and specifications so that industry can satisfy our needs with competitive, off-the-shelf products. This approach will be a cost-effective substitute for funding new development programs."

Specifying interfaces

To help push its programs along, the DOD has formed a subcommittee of the Defense Computer Resources Board to work on interface and requirements issues.

Called the Computer System Interfacing Working Group, its objective is to have the interfaces for the next-generation computers specified by mid-1987. "That's to give industry sufficient lead time to develop computers to begin qualification in early 1991 and to

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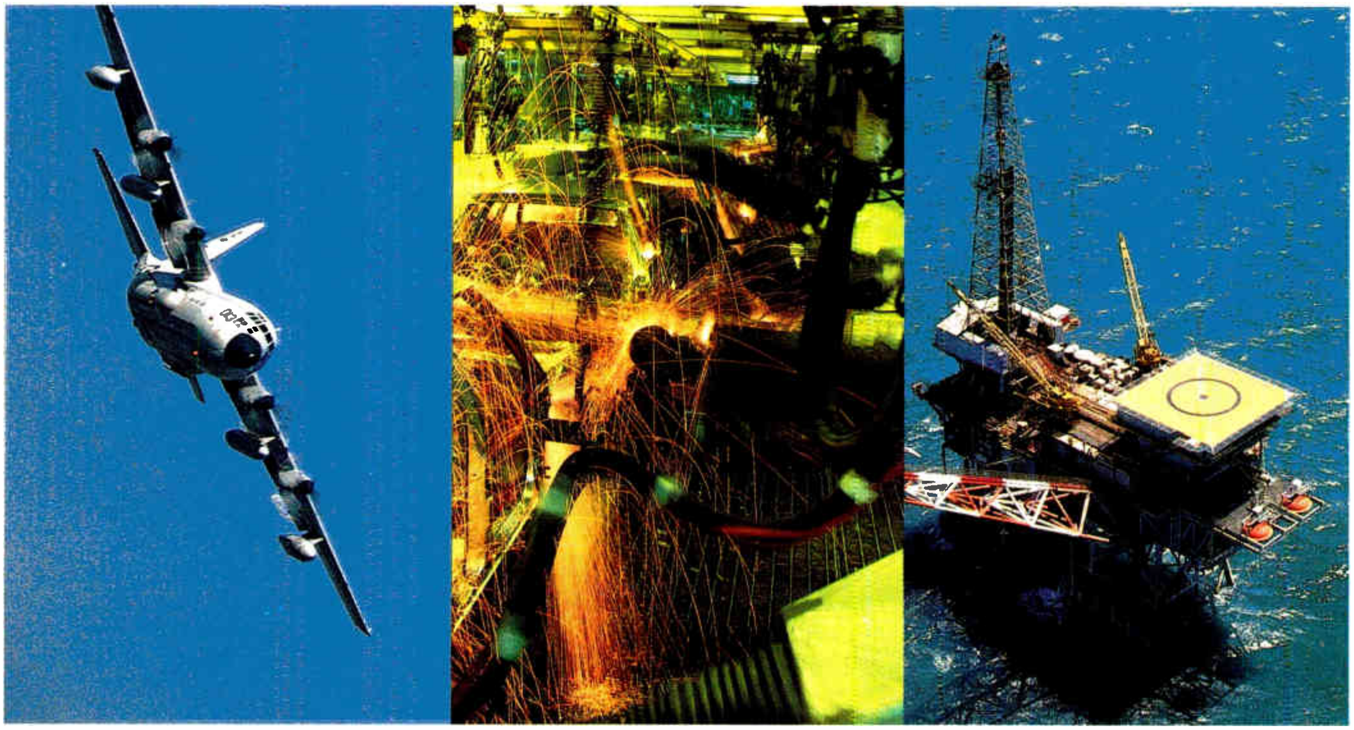

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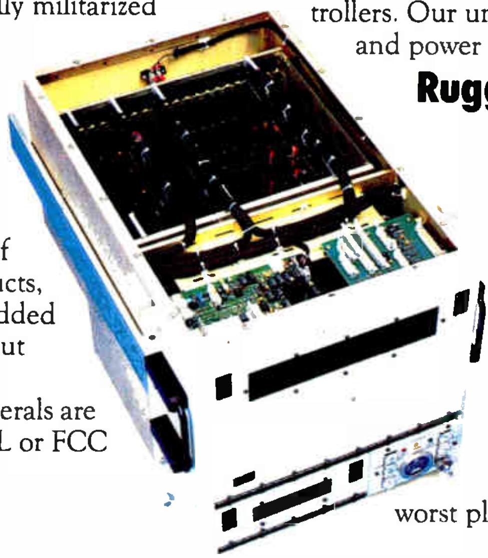

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enter service in new systems in the second quarter of 1992," said Hicks.

The DOD also continues to make progress with Ada, its standard programming language for mission-critical systems. It is now in use in 37 DOD projects, and the defense agency expects it to be included in 120 additional programs. Flight tests in the F-15 and F-20 have already demonstrated Ada's applicability to fighter control and avionics. Also, Boeing has announced Ada will be used in its future military aircraft. In addition, some artificial-intelligence systems have been developed using Ada. And the Federal Aviation Administration has adopted Ada for its upgrade program. It has also been approved as the standard programming language of the NATO alliance.

The Navy, meanwhile, is developing the Ada Support Environment, a formal program based on the Army system to get Ada into Navy systems. . It is using ALS/N, the Navy's Ada language, in its current generation of embedded computers—the UYK-43 and UYK-44—but expects to replace these systems with new ones by the mid-1990s.

Military AI

Military AI also continues to be a hot ticket, pulling down $95 million in industry revenue in fiscal year 1985, according to Frost & Sullivan Inc. Of that total, programs funded by the Defense Advanced Research Projects Agency accounted for an estimated $68.3 million, or 72% of the total military market. The New York market researcher says that total military funding for AI R&D exceeds the AI market because a substantial amount of the DOD funding supports in-house research in government laboratories, federal contract research centers, and universities.

Frost & Sullivan expects the military AI market to grow rapidly over the next few years, reaching almost $300 million in fiscal year 1990. Darpa's share of the market should decrease to about 67% in fiscal year 1990 as R&D work matures.

Excluding Darpa and Star Wars, the Air Force currently funds about half the military's AI programs, mainly in avionics. The Navy focuses its AI interests on mission planning, target acquisition, and combat control. The Army's AI programs are geared toward development of battle-management systems.

Star Wars redux

But it is Star Wars that takes the biggest chunk of the defense R&D budget; the administration plans to ask for $37.3 billion for basic and applied R&D covering prototype weapons and tracking, guidance, and battle-management systems over the next five years.

Star Wars got a big boost last month when two space vehicles launched by Delta rockets tracked each other until one homed in on the other and destroyed it. But software limitations could set the program back, as millions of lines of computer software code remain to be written and tested.

General-purpose computers and related products are also heading for a spurt in the military market. Roughly 45% of all computers used in the federal government are bought by DOD agencies. And the DOD plans to spend $7.5 billion this year for computer systems, including new bids for more than 40 major programs.

So far, the Army has been the slowest to adopt computer technology among the armed forces. Data published earlier this year by the Office of Technology Assessment, a Congressional support agency, credits the Army with only 9.6% of the total dollar value spent for data-processing equipment in the federal government, compared with the Navy's 15.1% and the Air Force's 18.6%.

But that's changing. The Army is "now the most active in purchasing computers," says Bob Dornan of Federal Sources. "The Air Force and Navy are spending a little bit more each year, but not that much. The Army seems to be really accelerating its spending."

The Army also is finally starting to think in terms of systems compatibility. The service, which now has over 145 different computers and 130 different languages, is working hard to narrow this to a single language and possibly a single computer system. It is also investigating trends in technology in memories, displays, printers, and communications, although its primary interest is processors, particularly 32-bit microprocessors. There is considerable interest among Army commanders in transportable, portable, and handheld computers in numbers necessary to equip not only the active Army but also the National Guard and Reserves.

The DOD currently requires computers with speeds in excess of 1 billion operations per second. Hicks also indicated that many future applications will require massive amounts of symbolic processing.

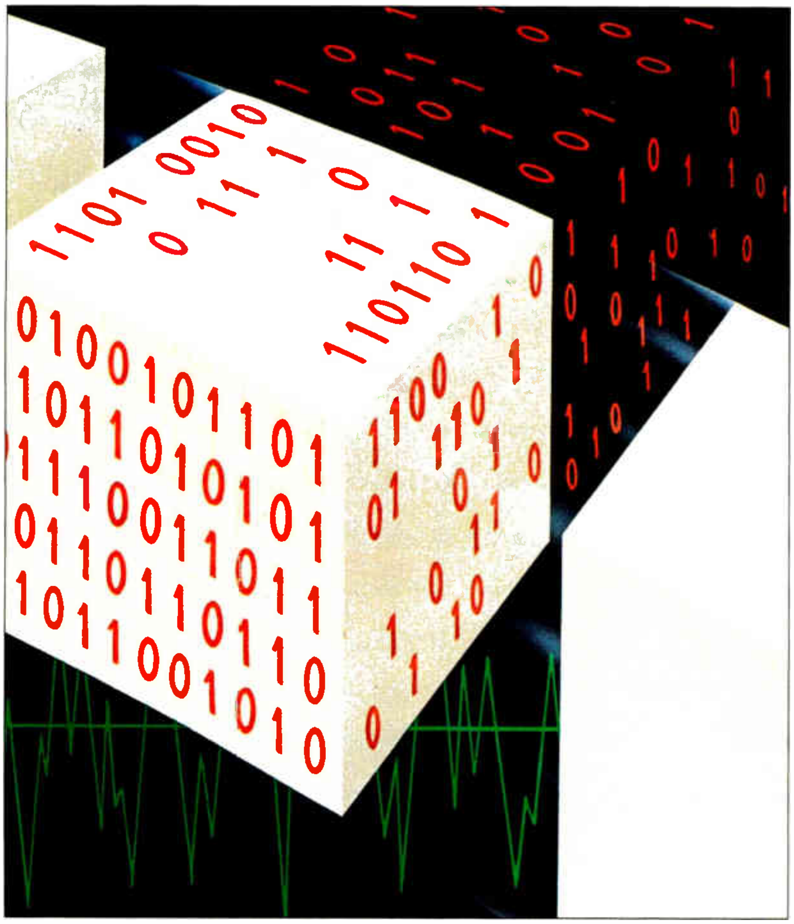
Where the military wants to cut costs is the collection and handling of technical data. The DOD spends $5 billion annually just to acquire and maintain technical data for weapon systems. So to streamline technical data bases and to improve communications with contractors, the DOD is sponsoring the Computer Aided Logistics Support program.

The idea is to create an integrated information processing system that will support virtually every existing defense logistics program. Manufacturers will use communications links to transmit documents, including engineering drawings, to the DOD for approval or changes, eliminating a great deal of paperwork at both ends.

In addition, the DOD is trying to put together an industrywide consortium to develop compatible DOD and industry computer architectures. "In an enterprise as large as DOD, we will always be faced with a mix of dissimilar equipment and software," says Deputy Defense Secretary Howard Taft IV. "We need interoperability for systems to complement one another in the exchange of information and so that we can upgrade systems or components without being locked into a single supplier."

Taft also says that the Pentagon wants to emulate industry in integrating computer-aided design and manufacturing systems. He cites a

DATA GRABBER.



Zoran's vector digital-signal-processing chip with 70,000 transistors requires only three instructions to do a 1,024-point fast Fourier transform in 2.4 ms.

"A speedy new single-chip contender is getting set to make a splash in digital signal processing. Zoran Corp.'s ZR34161 uses vector-handling techniques to gulp down blocks of data, rather than picking off a single data input at a time as scalar processors do. Vector processing alone is a big speed booster, and Zoran enhances it with embedded signal-processing algorithms that radically pare down system overhead.

The Santa Clara, Calif., company's 16-bit CMOS VSP is the first monolithic signal processor to utilize the powerful vector-handling techniques employed for scientific data processing in large vector computers and minicomputer array processors..."

Excerpted from an exclusive article in the July 24, 1986 issue.

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study by the National Academy of Sciences that showed companies with integrated CAD/CAM systems had cut their engineering design costs 15% to 30% and increased productivity significantly.

Another lucrative market awaits contractors that can manufacture Tempest-qualified equipment. Unlike conventional products, Tempest systems eliminate electromagnetic emissions, which unauthorized personnel can monitor to collect data from agency computers or computer peripherals.

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MILITARY TECHNOLOGY: MORE AMBITIOUS, MORE COSTLY

New technology is playing an ever larger role in military electronics. And as the multimillion-dollar high-tech projects, such as the Very High Speed Integrated Circuits program, the Defense Advanced Research Program Agency, and the Strategic Defense Initiative (better known as Star Wars), get even bigger, demand for such items as 1.25-μm chips and gallium arsenide devices will increase. Connectors also have become a hot military market.

DOD spending in fiscal year 1986 for electronics research and development was about $17 billion. That should remain stable for a while: in a report to the industry last year, the Electronic Industries Association's Government Division projected that the R&D budget for electronics would slip to about $16 billion by fiscal year 1989 and to $15 billion by fiscal year 1994. That report is scheduled to be updated later this month.

In an effort to speed up the VHSIC program, the Defense Department has signed advance agreements for chips with several VHSIC suppliers. The agreements, which require no competitive bidding, should pump millions of DOD dollars into new chip production. Several VHSIC program participants are ready to begin producing 1.25-μm ICs; volume production could begin by the end of this year. These Phase 1 chips already have been designed into several DOD systems.

Control Data Corp., Minneapolis, may have gotten a jump on other VHSIC producers with a radiation-hardened computer based on a 2-μm CMOS/silicon-on-sapphire process. The company's spacecraft control processor implements MIL-STD-1750A, the Air Force's instruction-set architecture for 16-bit computers. Computers designed to meet the rad-hard VHSIC-class 1750A standard aren't scheduled for delivery until 1989.

Prototype ready

Hughes Aircraft Co., El Segundo, Calif., has installed its Phase 1 chips in a prototype programmable electro-optical signal processor. And Harris Corp., Melbourne, Fla., will use $46.5 million from a VHSIC contract that runs through 1990 to develop a fabrication line for 0.5-μm, 100-MHz, Phase 2 CMOS ICs.

Also making noteworthy gains among military IC developers and users are GaAs chips, which are faster and use less power than silicon devices. Martin Marietta, Bethesda, Md., has formed a joint venture with Alpha Industries Inc., Woburn, Mass., to develop GaAs ICs for millimeter-wave radar. In addition, Honeywell, Rockwell International, Texas Instruments, and TRW have major GaAs development programs under way. Harris Semiconductor Group, Melbourne, Fla., has already introduced a line of 4-bit shift registers and other GaAs products.

Pentagon spending on GaAs is in the $135 million range. Darpa plans to supply the chips on boards to contractors that submit winning proposals for using the GaAs devices in a 32-bit reduced-instruction-set-computer chip set.

Despite its propensity forge ahead, the DOD has backed off its plan to develop multivendor interoperability under its Transmission Control Protocol/Internet Protocol (TCP/IP). Instead, it has turned over that responsibility to the commercial sector, hoping eventually to buy products off the shelf. TCP/IP is supported by more than 100 systems, and there's no lack of interest among private vendors to continue product development.

Micom-Interlan, Boxborough, Mass., recently began shipping a TCP/IP product for Ethernet. This Darpa implementation uses an intelligent front-end for high-performance file transfer and virtual terminal access for TCP/IP systems.

Strong sector

Connectors are another healthy sector: military/government markets should overtake the computer business for the first time this year as the top buyer.

ITT Cannon's Military & Aerospace Division, a leader in military applications, is working on several military designs, including flat-screen display connectors and the Army's armed decoy robotics development program, which is still in the R&D stage.

In addition, connector manufacturers will be trying to meet the Defense Department's still evolving MIL-STD-83527 for Arinc-type connectors. That standard is expected to require resistance to electromagnetic and radio-frequency interference as well as the ability to withstand higher vibration rates. ■

Such companies as Atlantic Research, Miltope, North Atlantic Industries, and Tempest Technologies specialize in ruggedized Tempest-qualified products for the military and U. S. intelligence agencies.

Nearly all developers of Tempest products sell directly to the military, but they also work with systems integrators. Recently, they have begun to align themselves with major systems manufacturers to expand their market base and jointly develop new products. Atlantic Research Corp., Alexandria, Va., has expanded its Tempest activities by acquiring Systematic General Corp., a Tempest manufacturer.

Tempest products now account for more than 25% of Atlantic Research's business, or more than $50 million annually. North Atlantic Industries Inc., Hauppauge, N. Y., will supply Systems Development Corp., a Burroughs company, with Tempest dot-matrix printers. And it will work on an original-equipment-manufacturer basis with MM/A-COM Information Systems Inc., which is supplying a variety of Tempest printers to the DOD. Potential revenue from these ventures over the next three years could come to $10 million, estimates Richard Berry, North Atlantic's vice president.

Relatively new to the Tempest market are Apple, Compaq, SASC Technologies, and Zenith. Apple Computer Inc., Cupertino, Calif., says it expects to introduce in the fall a Tempest-qualified Macintosh. Compaq Computer Corp., Houston, now has an IBM-compatible transportable personal computer, which was custom Tempestized by Loral. SASC Technologies, Vienna, Va., has an Air Force contract for 1,000 Tempest-qualified work stations. And Zenith Electronics Corp., Glenview, Ill., received a contract valued at about $242 million for 90,000 secure personal computers.

The need for data encryption and decryption has the Pentagon in the market for special computer systems and peripherals as well as for telecommunication hardware, including mobile and handheld radios and pocket pagers. The National Security Agency, which oversees most of the government's secure communications activities, has a program called Project Overtake under which it is working jointly with 11 private corporations to develop standardized off-the-shelf embeddable communications security modules.

It estimates that these standard modules will meet upward of 85% of all telecom equipment required for communications security. In the future, communication-system developers will just leave a space in their designs for the security module.

The NATO market

NATO represents yet another major market for vendors of military electronics, although it appears that more weapon systems will be purchased from European allies to correct an imbalance in NATO arms purchasing. A formal agreement reached late last year by NATO ministers said that "efforts to increase cooperation in research and technology, in particular to exploit emerging technologies, should be stepped up in order to achieve a more cost-effective use of resources of the countries of the alliance and to facilitate the establishment of cooperative projects."

A Frost & Sullivan report, "Military Systems Acquisition in the NATO Market," states that from 1985 through 1990, NATO will program and largely commit some $8 billion (1985 dollars) to meet its military requirements. It will spend nearly 40% of that on

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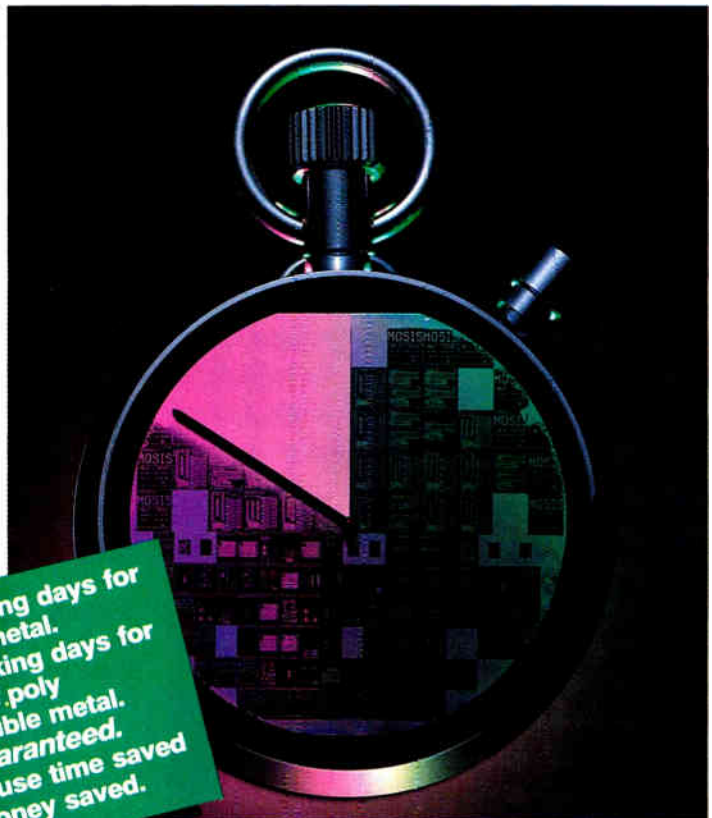

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command, control, communications, and information systems in contracts with companies from NATO countries. Taking the advice of the President's Blue Ribbon Commission on Defense Management, which earlier this year recommended cutting the cost and improving the efficiency of military procurements, the Pentagon has created a top-level position for supervision of military procurements. Expected to be confirmed as Undersecretary of Defense for Acquisitions is Richard P. Godwin, a longtime executive at Bechtel Corp. One of his first tasks will be to oversee the publication of new regulations governing the profits earned by military contractors. In effect, they will be paid more slowly and will be asked to bear more of the early costs of manufacturing weapons. Much of this plan is still in the draft stage, but it is scheduled to take effect next year.

Other key programs

Progress continues in other key programs as well. Having already spent more than $1 billion on the Very High Speed Integrated Circuits program, the DOD is beginning to see VHSIC Phase 1 chips designed in military systems. The program has contributed to several major industry developments, including the establishment of a number of high-technology integrated-circuit fabrication lines.

Similarly, the Darpa-supported gallium arsenide program is making headway. Prototype GaAs 32-bit reduced-instruction-set-computer chip sets should be delivered by mid-1988. The Henderson Electronic Market Forecast report projects market demand for GaAs products will grow to $5 billion in 1996 from current $240 million levels.

A little less exotic, perhaps, but still a strong category for many industry companies is the hybrid market. Though more than 300 companies are producing hybrid circuits, less than 50 are in the military market in a significant way, says Ron Huber, sales manager for CTS Corp.'s Microelectronics Division, a major supplier of hybrid circuits for the military, which accounts for about half its business.

The Defense Electronics Supply Center recently issued a new specification for military hybrids, MIL-STD-1772, which hybrid products must meet by the end of November to qualify for most defense programs. As of this writing, 13 companies have qualified, and about 30 are in the process of being qualified.

"Market research doesn't agree, but it's a growing market," says Huber. "The military market is the place to be." ■

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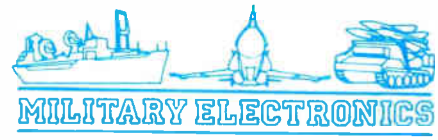

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Huge expenditures on defense software create demand for trained professionals

The way the Defense Department tells it, any software professional who would like to develop defense systems software has a job waiting, despite occasional layoffs by defense contractors in the hardware arena.

"Today, the demand for highly trained programmers, engineers, and managers exceeds the supply by 50,000 to 100,000," says Undersecretary of Defense for Research and Engineering Donald A. Hicks. "By 1990, we expect a nationwide shortage of over 1 million software professionals. In fact, if computer hardware continues its orders of magnitude progress in technology, it's not hard to envision the time when every man, woman, and child in the U. S. will need to be a programmer."

The Defense Department currently spends about $10 billion a year on defense software and expects this to exceed $30 billion a year by 1990. That would be more than 10% of the defense budget. More than 120 defense systems already under development are critically dependent on software; the DOD estimates the software requirement for these systems at about 150 million lines of code.

The DOD has developed several initiatives to lighten its software development burden. For one thing, approval of Ada as its standard programming language for mission-critical systems has improved productivity and simplified training and maintenance. The DOD also created the Software Engineering Institute at Carnegie Mellon University, Pittsburgh, to accelerate the transition of new software technologies from the laboratory to defense systems.

"It will improve the training of software professionals by enhancing the university software engineering curricula," says Hicks.

The Air Force's position, detailed at an American Defense Preparedness Association conference on military computers and software in Washington, is that military demands for software development in the U. S. exceed the capability of potential suppliers. Interservice competition for software developers and industry talent spread thinly among DOD contractors are the principal factors in the Defense Department's difficulties in obtaining and maintaining mission-critical software, the Air Force believes.

Air Force officials most concerned with the service's current and near-term requirements say that the government holds few forums on the acquisition of software-intensive defense systems. In addition, very few universities teach courses in software systems engineering. Both situations must improve if the DOD is to meet its rapidly growing software needs.

Soft, hard spots

Jobs in defense-work areas outside software development may wind up being harder to come by, however.

"The magnitude of the DOD's plans suggests many opportunities. But there's a lot of volatility in the market and uncertainty as well," says Jules Duga, a defense-electronics industry analyst at the Battelle Memorial Institute, Columbus, Ohio.

He says that defense electronics programs are, by nature, a matter of planned obsolescence. "So there will always be layoffs. The upside is that you can use in the commercial area what you learn in defense work. Some of the best people are working today in defense programs. Their technical skills are very good. If they want to make a move into nondefense work, they're usually in good shape."

Meanwhile, DOD spending remains fairly healthy in heavily computerized command, control, communications, and intelligence, electronics warfare, and simulation technologies. As a result, and because their own basic business is in a slowdown, several military airframe manufacturers are moving more into defense electronics, either by expanding and reorganizing their current operations or through mergers and acquisitions.

What new grads will find

This translates into a good overall job market for new electrical engineers, though not as good as it was two or three years ago.

The Engineering Manpower Commission of the American Association of Engineering Societies, Washington, which tracks enrollments, reports that the 1985 class produced 22,135 BSEEs, up 8% over 1984.

Preliminary data on salaries for 1986 BSEEs comes from the College Placement Council, Bethlehem, Pa. Its findings indicate an average starting offer of $27,804, up 1.5% over the year before. At the master's degree level, offers average $33,852, up 3.5%. PhDs are getting offers averaging $45,228, up 6.4%. The council's data indicates that computer-science majors at the bachelor's level received 2,644 job offers in July 1986 (31,728 computed on an annual basis), compared with 3,796 offers (45,552 on an annual basis) in July 1985.

The average salary offered to entry-level computer scientists in July 1986, according to the college council, was $2,216 a month ($26,592 a year) compared with $2,082 in July last year ($24,984 a year), for a 6.4% average July 1985 to July 1986 salary increase. ■

Electronics CAREER OPPORTUNITIES

Fall 1986 Planning Guide

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NEW PRODUCTS

MITEL FITS SPEAKERPHONE ON ONE ISDN PHONE CHIP

DSP ALSO HANDLES AUDIO SIGNALING AND TONE GENERATION

Any digital telephone circuit worthy of the name provides analog-to-digital pulse-code-modulation encoding. Now Mitel Corp.'s Semiconductor Division has taken a giant step beyond the norm with a low-power single chip that includes a fully functional speakerphone algorithm along with dual-tone multiple-frequency and tone-ringing generation.

"Most of our customers who've worked with digital telephone circuits before know it typically takes a codec, 12 to 15 MSI devices, and a digital telephone chip to build a functional phone," says Al Hawtin, Mitel's assistant vice president of component marketing. "Our design cuts the number of active circuits to two: the digital phone and some op amps."

ISDN PACKAGE. The new digital phone chip is part of Mitel's push into circuitry for the integrated services digital network. A total of 12 MSI, VLSI, and hybrid chips comprise the company's ISDN package, including a new S/T interface circuit.

"The power of ISDN is that it enables the user to access signaling," Hawtin says. For example, "with the scanning function, a digital telephone can be equipped with a display to show the calling party's phone number before the user actually picks up the phone."

Cramming so much functionality on a digital-phone chip took Mitel designers nearly two years, but since the company expects the digital telephone circuit market to hit a whopping $26.4 million next year, that investment of engineering time could bring a big payoff. Although Mitel is jealously guarding its market-share expectations, it anticipates avid interest when the chips become available in January for $31.95 apiece in lots of 1,000.

Two versions of Mitel's digital phone will be ready for sampling next week. The 8894 North American version implements μ-law companding, and the 8895 version implements Europe's A-law requirements. Mitel fabricates both versions with its proprietary CMOS process. Both measure 273 by 238 mils and operate at 5 V.

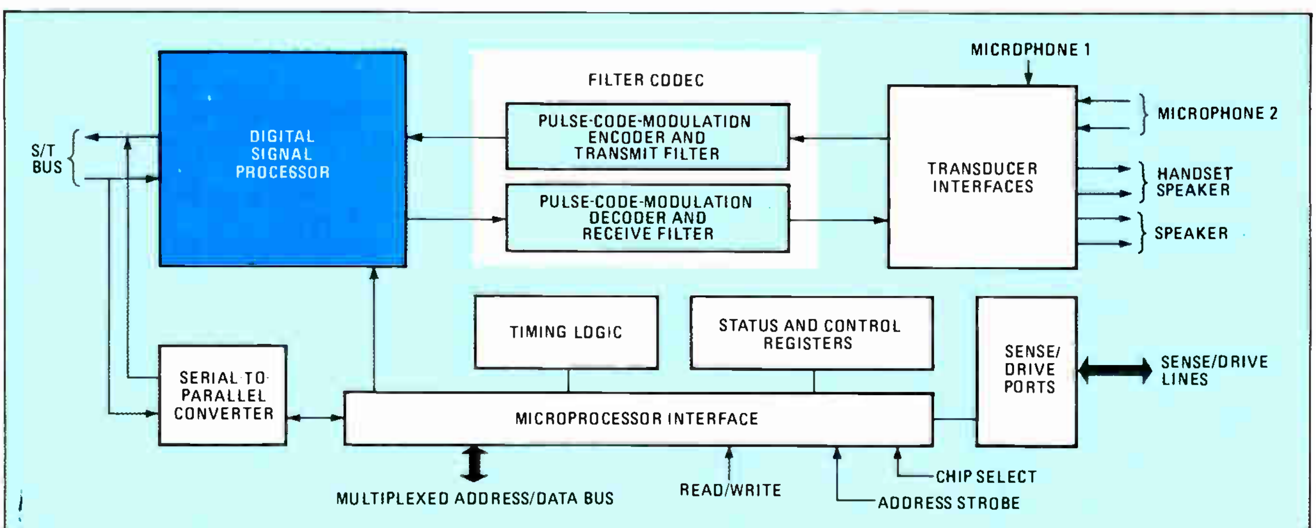
The chip's interfaces to telephone transducers, including the handset, microphone, and speaker, are standard and can be powered down independently under software control. Control by an external microprocessor is straightforward, because the microprocessor port on the digital phone accommodates Mitel's S/T-bus architecture, as well as Intel and Motorola microprocessors. The microprocessor can access seven sense/drive ports on the chip for keyboard input and display functions.

The heart of the 8894/5 circuit is a 4-MHz digital signal processor that executes three programs: the DTMF that produces audio signals from the phone's keypad; a tone generator that substitutes for a mechanical bell; and the speakerphone algorithm.

CUTTING NOISE. Mitel overcame an ambient-noise problem common to speakerphone circuits with a complementary arrangement that switches the gain control between the microphone receive path and the speaker transmit path. The DSP's algorithm determines which side of the transmit/receive path is active, based on the relative levels of the audio signal. It then boosts the gain along the active path in 2.5-dB steps, while the other path has maximum attentuation.

A detector algorithm determines if the audio signal is a voice or simply noise. If the receive signal has none of the characteristics of a voice signal, the algorithm adjusts the transmit-and-receive gain at mid-levels to balance for an idle state.

"There is nothing comparable to the 8894/5 on the market today," claims Hawtin. "AMD [Advanced Micro Devices, Austin, Tex.] is the only company making a concerted attempt to engineer a digital telephone circuit, and we think



WORKHORSE. Mitel's DSP executes three programs, including the DTMF generator that produces audio signals from the telephone's keypad.

they've taken the wrong approach. The AMD part has put both the digital telephone circuit and the ISDN S interface on a single chip. This limits its functionality—the S interface precludes its use in a proprietary PBX architecture."

OPPOSITE VIEW. Understandably, AMD disagrees. "The proprietary approach is what PBX manufacturers are providing today," says Ron Ruebusch, AMD's director of strategic marketing for communications products. "But we think there is going to be a sudden switch to ISDN, and we want to be well positioned for that switch."

Mitel's S/T interface, called the Subscriber Network Interface Circuit, conforms to CCITT 1430 recommendations. It handles full 192-kb/s signaling over a full-duplex, four-wire balanced transmission line using an alternative-space-inversion coding.

The on-chip high-level data-link controller handles the D-channel resource allocation and prioritization-of-access contention. Keeping the S/T interface on a separate chip allows manufacturers eager to market a fully functional desktop speakerphone or cellular phone the option to move quickly by adding two differential operational amplifiers, a handset, a microphone, and an audio speaker to the chip.

In the 8894/5 digital telephone chip, an on-chip filter codec handles the digital-to-analog and analog-to-digital conversion between the subscriber and the digital PCM switching system. The codec's receive and transmit filters both have programmable-gain controls that conform to the requirements set by the CCITT. *–Robert Rosenberg*

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Incorporating expert-system techniques, the product allows users to configure their network by answering a list of computer-generated questions about their equipment and requirements. The program, which is available for delivery now, is an optional subsystem for the company's standard 5000-series Network Management Systems and costs $15,000.

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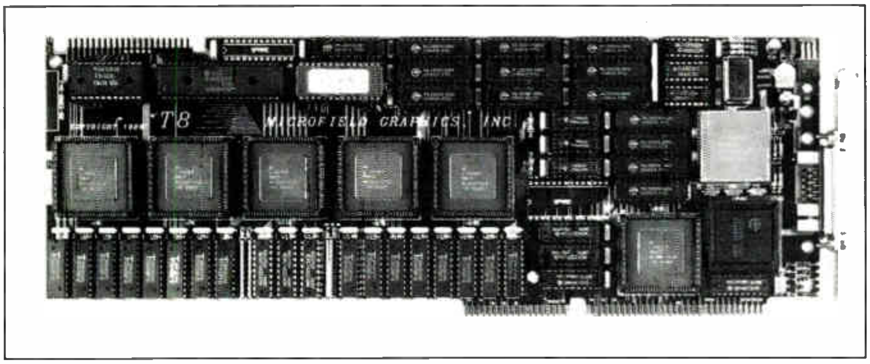


FIRM HOLD. Graphics card eliminates jerky motion when roaming large image data bases.

A general-purpose bit-manipulation computing engine called the Blit-slice dramatically speeds up the job of moving blocks of pixel data. Mounted on a high-performance, high-resolution graphics card for the IBM Personal Computer AT, it redraws graphics windows so fast they seem to pop instantaneously onto the screen. Users can also roam inside a large image data base without the jerky image movements characteristic of many systems. The Blit-slice is implemented in CMOS gate arrays.

Microfield Graphics Inc.'s T8 card brings this engine together with enough 1-Mb DRAMs—2 megabytes' worth—to accommodate eight graphics planes at a resolution of 1,280 by 1,024 pixels. The eight planes allow up to 256 colors to be displayed at once.

BIG HELP. The T8, which also carries its own 16-by-16-bit multiplier chip and a bit-slice drawing and emulation engine, can offload many tasks from the host processor, balancing the load in the graphics pipeline and eliminating processing bottlenecks. The board can handle data-transfer, command-interpretation, drawing, and window-manipulation operations, as well as image transforms, scaling, and clipping.

Technology advances on several fronts have made it possible for PC-based hardware priced at $10,000 or less to encroach on applications now claimed by costly high-end graphics systems, says Samuel Mallicoat, president of Microfield Graphics. The arrival of low-cost, high-resolution color monitors from NEC, Hitachi, and Mitsubishi is one major factor, he says. The growth in PC power is another, along with the availability of 1-Mb DRAMs.

The T8 fits into this trend, thanks to the performance and resolution it provides, but perhaps more importantly because of its high degree of application flexibility. The card is based on the microcode-driven architecture of the 2901 bit-slice processor family from Advanced Micro Devices Inc., so new microcode can be loaded into RAM to suit each application.

This flexibility allows the T8 to bring graphics-based applications to the PC AT from three different directions. The T8 can handle software adapted from programs running on personal computers, on work stations such as those from Sun Microsystems or Apollo Computer, and on high-end graphics systems using minicomputer or mainframe hosts and elaborate graphics terminals like the Tektronix 4125 or the IBM 5080. Applications thus can range from simple business graphics and computer-aided design, engineering, and manufacturing, to highly detailed mapping work.

Standard software for the T8 allows it to emulate IBM's Color Graphics Adapter—the first-generation graphics card for the PC—and also the IBM Enhanced Graphics Adapter, the higher-resolution card that is rapidly becoming a standard for PC graphics. The T8 is said to be the first AT-compatible card with its level of resolution to offer EGA emulation.

The card's standard software interface is a superset of the American National Standards Institute's Computer Graphics Interface definition. Enhancements facilitate window and text manipulation and the use of bit planes as logically separate drawing surfaces.

EASY CUSTOMIZATION. Primitives in the T8's standard software are fast enough for more than three-quarters of the applications currently being adapted to the board at beta sites, says Mallicoat. Furthermore, the command set can be easily customized with new microcode, and a programming tool kit and simulator are available.

Microcode can be developed, for example, to allow in-window emulation of graphics devices that are not already supported. And as processing bottlenecks are identified, microcode can be written to allow the T8 to help with specific tasks that relieve those bottlenecks.

One of the tools translates software that has already been adapted to the company's T4 graphics card, the T8's predecessor. P-CAD and Valid Logic are among the vendors of programs that currently run on the T4.

Three gate arrays were developed for the T8: a bus interface chip, another for address generation, and a third chip, four of which form the 64-bit-wide Blit-slice processor. Mallicoat credits these CMOS chips, along with the use of standard DRAM instead of video RAM, with keeping the board's power consumption down to 2.5 A at 5 V.

The T8 costs $4,500 in single units. Samples will be available by the end of the year; production quantities will be available in January. *–Jeremy Young*

Microfield Graphics Inc., 8285 S. W. Nimbus Ave., Suite 161, Beaverton, Ore. 97005. Phone (503) 626-9393 [Circle 340]

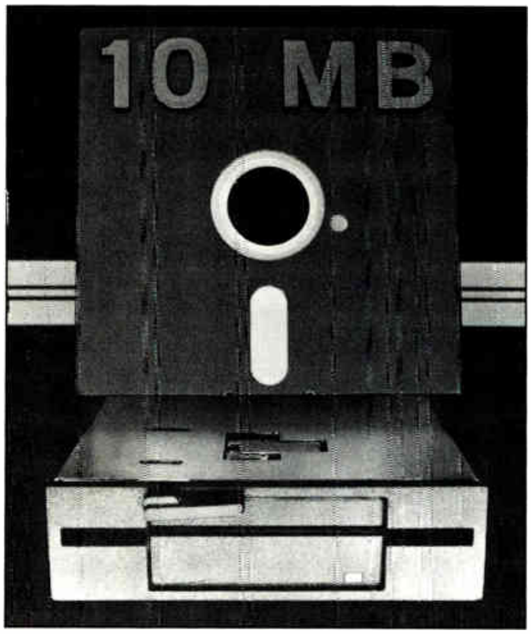
FLOPPY DISK DRIVE PACKS 10 MEGABYTES

By boosting capacity from 1.2 megabytes to 10 megabytes, floppy disk-drive makers are giving tape drives competition as the primary means of file backup for Winchester hard-disk drives on the IBM Personal Computer AT. The most recent entry is Konica Technology Inc.'s KT-510 half-high 5¼-in. drive that stores 10 megabytes unformatted on the 600-oersted floppy disk used by the IBM AT and compatibles. It will read—but not write on—IBM PC AT floppy disks.

The big boost in capacity means that the KT-510 can supplant more expensive tape drives as a backup for the PC AT. High-capacity floppy drives are not entirely new, but the competition is heating up. Eastman Kodak Co. introduced a 10-megabyte product based on 600-Oe media last year [*Electronics*, Nov. 25, 1986, p. 26], and Konica will soon announce a version that can read standard 300-Oe floppy disks from IBM PCs, PC/XTs, and compatible machines. Like its 600-Oe counterpart, it will not be able to write disks PCs can read. Future versions will offer higher storage capacity but will require higher-coercivity media. The company expects such products in two years.

MORE TRACKS. To achieve high storage capacity while retaining read capability on standard disks, Konica designed the KT-510 to write 480 tracks per inch—exactly five times the 96 tpi of a PC AT. It can still read conventional disks, however, because its read head looks for information where conventional heads would write it.

Not surprisingly, the new drive's tracks are considerably narrower—2.083 mils compared with 10.415 mils. The drive uses two systems to locate tracks: a sophisticated optical system for coarse positioning and an embedded closed-loop servo system for fine positioning. Using an embedded servo system means that the floppy media, while exactly the same as that of a PC, must have servo data written on it before being used in the Konica drive. The company has developed an inexpensive servo writer that media vendors can use for this purpose.



SPEEDY. Konica drive spins at 600 rpm—twice the speed of a conventional floppy—and has 5 times the tracks.

The lion's share of additional capacity comes from the fivefold increase in tracks. But some of the boost results from storing data on the tracks at twice the linear density of a PC AT floppy drive. As well as density increases, faster rotational speed helps boost data-transfer rates. The KT-510 turns at 600 rpm instead of the conventional PC AT disk's 360 rpm, and it boasts a transfer rate of 1.6 Mb/s, compared with 500 Kb/s on the standard PC AT floppy. The drive's average access time is 75 ms.

The drive is equipped with an SCSI Small Computer System Interface to mitigate differences in the transfer rates between the new drive and computer systems. Unlike other drives, the KT-510's SCSI controller switches between read and write operations without missing a sector.

Konica's drive will be available early next year for less than $400 in large quantities. Prototypes go on display at the Comdex Show in Las Vegas beginning Nov. 10. *–Jonah McLeod*

Konica Technology Inc., 777 N. Pastoria Ave., Sunnyvale, Calif. 94086.
Phone (408) 773-9551 [Circle 342]

PLUG-IN CARD TROUBLESHOOTS PC BUS

Personal-computer service technicians confronted with a blank screen or a balky machine that won't boot a software diagnostic program no longer have to reach for their probes and oscilloscopes. Using a bus-based approach to diagnosis, the Crowcard from Applied Physics Inc. is billed as a low-cost way to save time in pinpointing problems on the IBM PC, PC/XT, and compatibles. It is designed for use by PC service companies, repair shops, companies that do in-house maintenance, and trade schools.

The Crowcard is built on a standard printed-circuit card and contains circuitry for monitoring I-bus activity of a PC or PC/XT. A series of 50 light-emitting diodes on the card correspond to the 50 bus lines monitored, including supply voltages, address and data, system clock, input/output, memory, interrupt, and direct-memory access lines. The LEDs are red or amber and are grouped according to function.

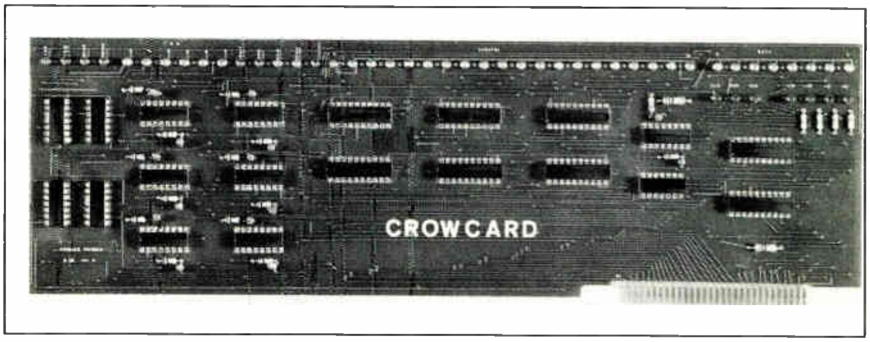
After plugging the Crowcard into an expansion slot, the technician begins to exercise the machine. He can get a quick clue to the problem by observing the LEDs. The failure of a particular interrupt request to energize the appropriate LED, for example, indicates a problem with that function. Depending on the function monitored, other LEDs should remain lit if the function is working properly.

Once the Crowcard pinpoints problems on a particular line, the technician can use probes and a scope to investigate the problem. Or, he may insert a new board in the machine and tag the bad one for further analysis by his repair shop, based on clues provided by the Crowcard. In either case, the Crowcard can save time—perhaps as much as an hour in some cases—by telling the technician where to look, says David Doty, Applied Physics vice president and general manager.

Until now, the alternatives have included unguided probing or using microprocessor-based board analysis systems that typically cost several thousand dollars, he says. By contrast, the Crowcard costs $249 each in quantities up to four. Discounts range up to 40% for orders of 50 units or more.

NO ANALYSIS. Doty concedes that the use of diagnostic software, when possible, is preferable to the Crowcard for pinpointing PC problems. The Crowcard has no analysis capability, but fills a need, he argues. "People can have all the diagnostic software in the world, but if the machine is dead, it won't do them any good."

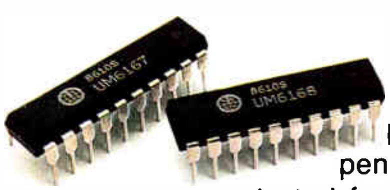
The Crowcard was developed at Purdue University by Brandon Crowe, Applied Physics president, to fill a need in Purdue's PC maintenance program. Applied Physics was incorporated last month and is funded by a venture capi-



FLASHY. Crowcard's LED display helps PC technicians diagnose trouble.

Score A Winning Touchdown with UMC

With backing from UNITED MICROELECTRONICS CORPORATION, one of our customers scored a winning touchdown with a voice control IC last year. He netted a profit of 2.5 million dollars on just one product. This is one of the many examples of how UMC helps its customers score financial goals.



UMC scored its first touchdown by becoming profitable 6 months after it went into operation and has been making a profit and registering phenomenal sales growth annually since then. Last year, 4 quarters of penalties left most companies sitting on the bench and several others were ejected from the game. UMC, however, still romped to a sales growth rate of 24.4%, which was the fourth best in the world and outscored 92% of the IC industry.

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tal organization that is associated with the university. The company is marketing the Crowcard under license from Purdue, and is also planning another, enhanced version of the product early next year, the Crowcard II. That product will monitor 86 bus lines and will be designed for use with the expanded bus used on the IBM PC AT and compatibles. Crowcard II is planned for February availability. The Crowcard is available now. *–Wesley R. Iversen*

Applied Physics Inc., 1291E Cumberland Ave., West Lafayette, Ind. 47906.
Phone (317) 497-1718 [Circle 341]

OPEN ARCHITECTURE EASES UPGRADING

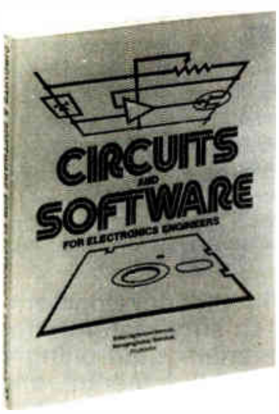
A voracious appetite for the latest technology in high-resolution graphics, blazing processors, and massive data storage keeps the makers of computer-aided oil exploration tools hunting for ways to upgrade their systems without reconfiguring them. That's why Landmark Graphics Corp., a leader in configuring computer systems that help geophysicists systematically process and graphically display mountains of seismic data, is introducing an open-architecture IBM RT Personal Computer-based Unix work station it characterizes as a major step forward for its "anti-obsolescence" campaign.

The Landmark Desktop Workstation's price makes it a comfortable fit for projects that involve representing seismic data in two dimensions or small portions of three-dimensional interpretation projects. It will cost $65,000, not including software, and will be available next month.

For bigger jobs, the company will introduce the $200,000 to $300,000 Landmark IV in the first quarter of 1987. Complementing the Desktop Workstation, this top-of-the-line open-architecture offering will feature a Unix operating system and an Intel 80386 microprocessor to boost performance over the Intel 80286-based Landmark III.

In the standard configuration, the Landmark Desktop features a 16-in. monitor, 1,280-by-1,024-pixel graphics resolution, 330 megabytes of hard-disk memory, and a mouse. Thanks to the IBM RT PC's 32-bit central processing unit, it runs at a maximum rate of 1.8 mips. The Desktop supports Ethernet and DECnet networking protocols and IBM's Token Ring networking scheme.

Landmark opted for an open-architecture strategy to take advantage of new technology as it becomes available, says marketing director Lisa Chiranky. The



Houston-based firm was among the first to implement optical-disk storage, for example, and to offer high-resolution hard copy. "In order to get new technology, other vendors will have to change their platforms," she says.

The company chose IBM's version of the industry-standard Unix System Version 2 and is adapting its entire set of oil-exploration application software to operate in a Unix environment. The company has developed a range of database, mapping, graphics, and interpretation software in-house and has authorized some third-party software development.

Software packages generated by Landmark cost $60,000 to $80,000. Third-party software packages cost $20,000 to $30,000. *–Jack Shandle*

Landmark Graphics Corp., 1011 Highway 6 South, Houston, Texas, 77077.
Phone (713) 531-4080 [Circle 343]

TAPE CARTRIDGE HALVES DATA LOSS

A ¼-inch-tape data cartridge for tape drives that will work with the new QIC-120 recording format or future high-density recording technologies has less than half the data dropout of conventional media, according to its maker, Data Electronics Inc.

The Series II family uses a new tape formulation with an improved tape-guiding system to improve data integrity. Instead of the conventional ¼-in. tape formulation, DEI uses a "plated" media technique that doubles longevity and significantly lowers wear on the recording heads.

Mechanical tape guiding is improved through use of a longer-lasting textured belt, a one-piece tape guide that minimizes tape skew and secures rotating components. The decay-resistant textured belt is said to maintain tension up to five times longer than conventional belts. The stable belt tension improves tape speed control and data recording integrity, and reduces the torque necessary for tape drives to spin the hub. The Series II family uses one-piece guides to control lateral skew. Available now, the cartridge's prices range from $31.50 to $49.50 each.

Data Electronics Inc., 10170 Sorrento Valley Rd., San Diego, Calif. 92121.
Phone (619) 452-7840 [Circle 351]

PC CLONE BOASTS TWO CLOCK SPEEDS

An entry-level addition to the PC market offers two clock-rate operating modes, built-in display capability, a choice of keyboards, and a single floppy-disk drive for $1,265. Standard features on

the WYSEpc+ include: 9.54-MHz and 4.77-MHz clocks; a monochrome/color graphics adapter; a 256-K-byte CPU board, expandable to 640-K bytes of RAM; two serial ports and one parallel port; a real-time clock with battery back-up; and a choice of IBM PC AT-style or enhanced-style keyboards.

Graphics capabilities are compatible with IBM monochrome and color graphics adapters, the Hercules monochrome graphics adapter, and many other adapters. The built-in adapter provides 16 shades of gray and a variety of screen resolutions, including 132 columns by 44 lines, and flicker-free scrolling.

The WYSEpc+ can also be configured with two floppy drives for $1,445 or a 20-megabyte hard disk for $1,995. All are available now.

Wyse Technology, 3571 N. First St., San Jose, Calif. 95134.
Phone (408) 433-1000 [Circle 352]

PROCESSOR FREES I/O BOTTLENECKS

The high throughput capabilities of the current generation of microprocessors have made it difficult for I/O subsystems to keep pace, but Intel Corp.'s UPI-452 programmable I/O processor family is aimed at breaking that bottleneck. These VLSI devices incorporate a sophisticated buffer that allows host processors to communicate with peripherals in data bursts instead of bytes.

For high-speed interface to such processors as Intel's 80286 microprocessor, the UPI-452 combines onto a single chip a 128-byte, bidirectional first-in first-out buffer; a two-channel direct-memory-access processor; an 8-K-byte EPROM; 256 bytes of RAM; and an MCS-51 microcontroller with 40 programmable I/O lines. Each of the FIFO channels is user-programmable for size and threshold. The buffer supports three slave/bus-interface handshake conventions.

Available now in sample quantities, Intel offers the UPI-452 in EPROM, ROM, and external memory versions. Production quantities will be available in November. In lots of 1,000, the EPROM version will sell for $70 each; the external-memory version will cost $30 each.

Intel Corp., Literature Dept. W-319, 3065 Bowers Ave., Santa Clara, Calif. 95051.
Phone (916) 351-5173 [Circle 353]

REGISTER-FILE IC BUILDS SPEEDY SCRATCH PAD

AMD's SINGLE CHIP CAN REPLACE UP TO EIGHT ECL RAMs AND WILL PROVIDE 20% FASTER ACCESS TIMES

Speedy scratch-pad memory, which keeps data flowing to high-performance computers, will run faster and use less board space with a new single-chip, four-port register file from Advanced Micro Devices Inc. The 120-pin Am29434 is the first device in an AMD 32-bit-processor chip set made in emitter-coupled-logic technology.

Having an area of 65,000 mils^2, the 29434 64-by-18-bit register file contains two write and two read ports for data, along with four 6-bit ports for addresses. The chip has an access time of 20 ns and is able to perform two reads and two writes in a single cycle. Also, 29434 devices may be cascaded together to provide either wider word widths or deeper register files without speed loss.

LESS DELAY. Before the advent of this dual-access four-port register file, equivalent scratch-pad memory subsystems had to be made with ECL random-access memories and discrete logic or gate arrays, says Bob Tabone, directorate marketing manager for microprogrammable-instruction-set processors in San Antonio. "Even though you can get ECL RAMs with 10-ns speeds, you end up adding off-chip delays between the parts. That's what makes our part so competitive," he adds.

An equivalent scratch pad made with eight ECL RAMs and other necessary logic would top out at a 25-ns access time, 5 ns slower than the 29434, says Tabone. It would also occupy about three times as much board real estate.

Tabone says the growing use of ECL gate arrays inside minicomputers and mainframes is creating a demand for fast scratch-pad memories. Aimed at that design niche, the 29434 is targeted at a broad range of commercial applications, including large computers, telecommunications equipment, high-end graphics, array processors, and test systems. AMD is also considering a military version of the register file.

ERROR GUARD. The 29434 also contains extra bits for byte-parity, which may be used to detect errors and provide data security. It supports the fault-detection scheme of AMD's Am29423 ECL 32-by-32-bit parallel multiplier, which will be introduced in early 1987. Together they will provide 50-ns cycle times.

The 29434 register file may also be used with other microprocessors. A single-phase clock input helps ease timing controls for write-enable and read-write multipliers on-board the register file, Tabone says. The 29434 operates over a standard temperature range of 0° to 70° C, dissipating a maximum of 4.9 W. The 29434 is processed in AMD's ion-implanted oxide-isolated stepper technology, known as IMOX-S II, which produces 2-μm feature sizes and 4-μm metal pitch.

The part operates from a standard power supply of +5 V. Housed in a ceramic 120-pin grid array, the 29434 sells for $180 each in 100-piece quantities. *–J. Robert Lineback*

Advanced Micro Devices Inc., 901 Thompson Place, P.O. Box 3453, Sunnyvale, Calif. 94088.
Phone (512) 647-6243 [Circle 360]

EPROM TOLERATES WIDE SUPPLY RANGE

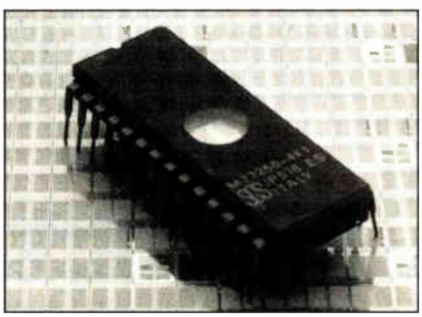
Operating at a 10% tolerance for battery-operated systems that need to accommodate wide power-supply ranges, National Semiconductor Corp.'s 512-K CMOS EPROM offers access times of 250, 300, and 350 ns.

Fabricated in National's microCMOS double-polysilicon technology, the NMC-27C512 consumes only 55 mW in the active mode. Packaged in a 28-pin ceramic DIP with an ultraviolet-light window, the device is available now and is priced from $25 to $30 each in quantites of 100, depending on speed.

National Semiconductor Corp., 2900 Semiconductor Dr., P. O. Box 58090, Santa Clara, Calif. 95052.
Phone (408) 721-4407 [Circle 365]

256-K EPROM HAS 200-ns ACCESS TIME

A 256-K ultraviolet-erasable PROM featuring 200-ns access times and a single 5-V power supply is well suited for use



with microprocessors that have 1-megabyte addressing capabilities, such as Zilog Corp.'s Z family. In standby mode, the TTL-compatible chip reduces power use by 60% without increasing access time. The active current is 100 mA; maximum standby current, 40 mA.

The M27256 EPROM's large storage capacity can accommodate entire operating systems, diagnostics, high-level language programs, and specialized software on a system's memory bus to avoid time-consuming disk accesses and downloads.

The M27256 is organized as 32-K words by 8 bits and is manufactured with SGS Semiconductor's proprietary n-MOS process. Available now, the chips cost $5.14 each in lots of 1,000. Other models access in 250, 300, and 450 ns.

SGS Semiconductor Corp., 1000 E. Bell Rd., Phoenix, Ariz. 85022.
Phone (602) 867-6100 [Circle 370]

FOUR-CHANNEL DMA IC ARRIVES IN CMOS

Oki Semiconductor Corp. has introduced a CMOS programmable direct-memory-access controller that is a pin-for-pin replacement for its n-MOS DMA part. Compatible with TTL devices, the CMOS version, M82C37A-5, handles four independent channels and completes the set of peripheral chips supporting the company's 80C85A-2 and 80C88/80C86-2 versions of Intel microprocessors.

The device transfers data at speeds up to 5 MHz without intervention of the CPU. It can operate independently to enable or disable any of its four channels and can automatically initialize each channel independently. The channels have full 64-K word-address and word-count capability. If more than four channels are needed, the device can be cascaded.

Speed-enhancing innovations include designating channels for pseudo-transfers, a technique that allows data to bypass the controller via the system bus, and a compressed-timing capability for the controller. While operating at 5 MHz, power consumption is less than 50 mW and drops to less than 500 μV in the standby mode.

Available now, the controller costs $14 each in lots of 100.

Oki Semiconductor Inc., 650 N. Mary Ave., Sunnyvale, Calif. 94086.
Phone (408) 720-1900 [Circle 366]

TI OFFERS LOW-POWER ANALOG SWITCH ICs

Two monolithic chips from Texas Instruments Inc. that are designed to switch analog or digital signals feature four bilateral input-enable switches, which are actuated by logic or high-voltage

signals. Applications for the chips include signal gating, chopping, signal multiplexing, and analog-to-digital or digital-to-analog conversion.

Fabricated in LinCMOS technology for low power consumption and low on-state impedance, the chips can switch analog or digital signals with amplitudes up to 12 V in either of two directions. The TLC4016 has a 62-ns delay in 2-V supply operation; the TLC4066 has a propagation delay of 30 ns. Otherwise, their specifications are identical. Typical on-state impedance is 30 Ω with 12-V supplies and 50 Ω with 9-V supplies. Cross-talk attenuation between any two switches in a package is 50 dB at 1 MHz.

Texas Instruments Inc., Semiconductor Group, P. O. Box 809066, Dallas, Texas 75380. Phone (800) 232-3200 [Circle 367]

TINY 12-BIT DACs ARE PRECISE TO ±0.5%

Dual 12-bit digital-to-analog converters that occupy one-half the space of two separate 12-bit DACs have been introduced by Analog Devices Inc. They feature ladder-resistance matching and DAC tracking that is precise to within 0.5%.

The AD7537 and AD7547 each contain two 12-bit current-output DACs on a single chip, but the AD7537 adds features such as double buffering of data inputs to allow the simultaneous update of both DACs on the chip. Packaged in 0.3-in.-wide 24-pin DIPs, both devices are the smallest available, according to the company.

The AD7537's 2-byte, 8-plus-4-bit input structure facilitates right-justified loading from an 8-bit bus. The AD7547's parallel-loading structure allows data loading of one 12-bit word from a 16-bit bus. Applications for the dual DACs include automatic test equipment, programmable filters, process control, and space-sensitive designs. Samples are available from $14.50 in lots of 100.

Analog Devices Semiconductor Co., 70 Shawumt Rd., Canton, Mass. 02021. Phone (617) 935-5565 [Circle 368]

CMOS IC DRIVES LCDs AND OTHER DISPLAYS

Liquid-crystal displays can now be driven directly with a CMOS decoder/driver that includes latches for storing binary-coded decimal data and turning off (blanking) the seven segments that make a digit. RCA offers two versions of the device: HC for new all-CMOS designs; and HCT, which is pin-compatible with low-power Schottky TTL logic.

Coded CD54/74HC/HCT4543, the device contains an active-high disable input, an active-high blanking input, and a phase input used to drive LCDs with a square-wave signal. Besides driving LCDs directly, the device can drive incandescent, fluorescent, or gas-discharge displays if used with a current amplifier. Packaged in 16-lead DIPs, the HC version costs $1.14 each in 100-piece lots; the HCT $1.98 each. Available now, they come in other popular packages.

RCA Solid State Division, P. O. Box 2900, Somerville, N. J. 08876.

400-MHz OP AMP AIDS FLASH ADCs

A monolithic bipolar high-performance operational amplifier with a unity gain bandwidth of 400 MHz from Plessey Semiconductors is designed as a companion for high-speed flash analog-to-digital converters but is also appropriate for other circuits, even those with low impedance and high capacitive loads.

The SL9999 features programmable open-loop gain with a gain-bandwidth product of 2 GHz at 20 dB. Output current can be programmed to any level from −50 to +50 mA. A nonsaturating amplifier, the SL9999 has a typical slew rate of 1,000 V/μs. The company says the chip demonstrates that fast bipolar silicon devices compare favorably with GaAs technology. Available now in 16-pin in-line ceramic packages, the chip sells for $13.20 each in lots of 1,000. A leadless chip carrier version will be available later this year.

Plessey Semiconductors, 3 Whatney, Irvine, Calif 92718. Phone (714) 951-5212 [Circle 371]

HITACHI 1-Mb EPROM PROGRAMS IN 14 S

A 1-Mb ultraviolet-erasable PROM from Hitachi America Ltd. features a 14-s page-mode programming time—faster than many 64-K EPROMs—without sacrificing data retention or programming depth, the company claims.

The device comes in two versions: the 32-pin HN27C101G and the 28-pin mask-ROM-pinout HN27C301G. Fabricated in the company's 1.3-μm CMOS process, they both have 200-ns access times and low standby current.

Maximum operating current for the part is 30 mA, and its maximum standby current is 20 μA. It can be programmed four bytes at a time instead of one byte at a time, and boasts a programming-pulse period of only 0.2 ms.

Hitachi America Ltd., 2210 O'Toole Ave., San Jose, Calif. 95131. Phone (408) 435-8300 [Circle 372]

HP's INDUSTRIAL TERMINAL FEATURES TOUCHSCREEN

COLOR DISPLAY SEEN AS ALTERNATIVE TO LED SCREENS IN HEAVY-INDUSTRIAL ENVIRONMENTS

HARD-HAT INTERFACE. Rugged, sealed unit has high-resolution graphics and is easy to use.

An industrial-control terminal designed for factory-floor workers with little or no computer experience has a rugged touchscreen monitor and full-color capability to make it easier for the workers to use it, according to Hewlett-Packard Co. The HP9666A Operator Interface Unit (OIU) has a 12-in., high-resolution display. Its interactive touchscreen is sealed in a dust- and drip-protected enclosure.

"The target application is for heavy manufacturing environments," says Rich Williams, a Hewlett-Packard product manager and one of the unit's designers. "We see it as an alternative to standard LED flat-type displays in an environment where an ordinary computer terminal isn't going to survive," he says. The OIU can operate in temperatures from 0° to 60° C (32° to 131° F), and contains an internal fan for ventilation and heat dissipation.

FULL COLOR. One of the unit's strongest features, says Williams, is its full-color graphics capability. With a 64-color palette, customers can choose eight colors, or even mix their own shades. The OIU will also interface with H-P 1000, 3000, and 9000 computer systems, and can support graphics software from independent vendors.

The unit is easy for factory-floor workers with little or no experience with computers to operate. The company's touchscreen technology uses a sealed infrared touch bezel, and can be used for alphanumeric or graphic applications. By touching the screen, an operator can perform simple on/off functions or more complex tasks, such as display and control of industrial processes.

In addition to the touchscreen, the unit is equipped with a sealed-membrane Qwerty keyboard with eight user-definable keys, a bar-code reader, a mouse, and a graphics tablet. Two RS-422 and RS-232-C ports enable input and hard-copy devices to be connected at the terminal location.

Hewlett-Packard has big plans for the 9666A. "In terms of price and performance, no one can touch us," says Williams. Orders have already been placed by two major automakers, a food processing plant, a chemical plant, and a paper mill.

The unit is available now at a base price of $6,300 in quantities of 10 or fewer. There is a 5% discount for larger quantities. The optional bar-code reader costs $600; a tilt/swivel kit, $425, and a rack-mounting kit, $230. *–Rick Elliot*

Hewlett-Packard Inc., Advanced Manufacturing Systems Division, 11000 Wolfe Rd., Cupertino, Calif. 95014.
Phone (408) 725-8111 [Circle 460]

CONTROLLER LINKS PCs TO MAP LANS

A communications controller transforms IBM Personal Computers into industrial work stations on a local-area network operating under the Manufacturing Automation Protocol 2.1, executing all seven layers of the MAP specification and supporting up to eight simultaneous connections.

The MAPware Series 1200 controller card from Concord Communications Inc. represents the first generation of low-cost MAP interfaces, the company claims. Applications developers can interface the LAN at the session, transport, or data-link layers. Using a single slot on the computer backframe, the card connects PCs, PC/XTs, and PC ATs to the LAN via broadband or carrier-band modems. Concord's 10-megabyte/s broadband modem is software-adjustable for frequency and for modem transmit power levels. Its 5-megabyte/s carrier-band modem meets the IEEE 802.4-B proposal for phase-coherent frequency-shift keying. Including modem and software, the unit costs $2,695. It will be shipped during the first quarter of 1987.

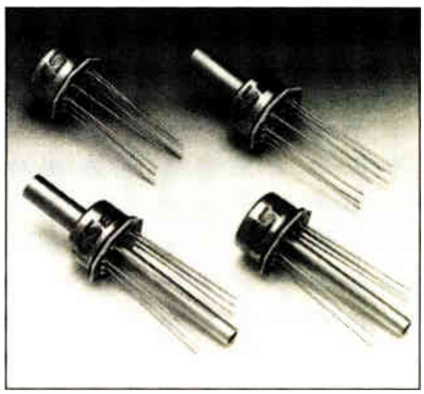
Concord Communications Inc., 397 Williams St., Marlboro, Mass. 01752.
Phone (617) 460-4646 [Circle 464]

SENSOR MEASURES LOW PRESSURES

IC Sensors Inc. of Milpitas, Calif., has introduced a solid-state pressure sensor accurate to ±0.15 in. of water at 2 lb/in.^{2} for gases and many liquids, including acids and solvents.

Capable of measuring gauge and differential pressures, the sensors are available in four different TO-8 packages and come in 40 graded models. All can be mounted on pc boards and are compatible with existing TO-8 packages. Built with piezoresistive IC technology, the sensors operate between –55° and +125° C. Outputs range from 15 mV per lb/in.^{2} to 70 mV per lb/in.^{2} at 1.5 mA excitation current. Their low-noise characteristics make them suitable for high-gain amplifiers. Applications include filters and filtering systems, pressure switches, and environmental control systems. Available now in 40 models, the sensors cost $17 each in lots of 1,000.

IC Sensors Inc., 1701 McCarthy Blvd., Milpitas, Calif. 95035.
Phone (408) 946-6693 [Circle 466]



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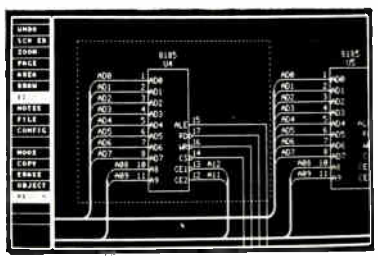

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ELECTRONICS WEEK

SIEMENS FAVORED AS BUYER FOR CGCT

Siemens AG is reportedly on the inside track in negotiations to gain control of Compagnie Générale des Constructions Téléphoniques, the French communications firm that boasts about 16% of France's market for public switches. French officials are said to favor a Siemens-CGCT alliance to counterbalance the linkup between Compagnie Générale d'Electricité and ITT Corp. [*Electronics*, July 24, 1986, p. 113] and to help remove German fears of a powerful CGE/ITT combine.

COMPATIBILITY KEY TO EUROPEAN CO-OP

Eight European computer makers have set up a joint company to ensure compatible operating standards for their data-processing and office-automation equipment. Named SPAG Services SA, (for Standards Promotion and Application Group), the company was established in Brussels late last month by Bull SA and the Thomson Group of France, Britain's International Computers Ltd., STET and Olivetti of Italy, Philips International NV of the Netherlands, and a pair of West German players, Nixdorf Computer AG and Siemens AG. SPAG will monitor these companies' compatibility with the Open Systems Interconnection reference.

AMD SHAKES UP MANAGEMENT

Advanced Micro Devices is shaking up its top management team. Chairman and chief executive officer W.J. Sanders III is relinquishing the company's presidency to executive vice president Tony Holbrook, who currently directs day-to-day operations. The Santa Clara, Calif., chip maker says the move formalizes the executives' current duties and is not related to AMD's recent financial difficulties. Suffering from four straight losing quarters and expecting a fifth, AMD says it is writing off a $15 million to $20 million loss for discontinued wafer-fab facilities.

SYMBOLICS CUTS PRICES UP TO 33%

Growing competition is forcing Symbolics Inc., a builder of artificial-intelligence computer systems, to cut some of its prices between 28% and 33%. The reduction applies to the Symbolics 3610 AE applications delivery system and two of the company's entry-level development systems. The Concord, Mass., company says gate-array technology and larger-scale production have reduced manufacturing costs. Nevertheless, hurt by competition from Texas Instruments Inc. and Digital Equipment Corp., Symbolics anticipates a loss in the current quarter.

NATIONAL TURNS PROFITABLE . . .

The National Semiconductor Corp., Santa Clara, Calif., declared a $5.7 million profit for the first quarter of its 1987 fiscal year—a considerable improvement over the $54.3 million operating loss it had for the same period a year ago. Sales were up nearly 23% to $501.1 million from $408.8 million in 1986. Most of the increased sales came from the Advanced Systems Group, which markets mainframe computers, and the Datachecker group; but even the Semiconductor Group reported a small sales increase—the first in more than a year.

. . . AND SIGNS WITH FOREIGN PARTNERS

Seeking to expand its markets, National Semiconductor is entering strategic partnerships with two foreign firms. National is joining with France's Thomson Semiconducteurs to develop telecommunications products, and with Japan's NMB Semiconductor Co. to develop advanced VLSI circuits. National denied that the Japanese agreement included production of dynamic random-access memories, an NMB specialty, dousing speculation on this subject.

GE, RCA COMBINE CHIP OPERATIONS

The marriage of RCA Corp.'s Solid State Division and General Electric Co.'s Semiconductor Business Division is shaping up, and RCA is faring much better than many expected. RCA says vice president and general manager Carl Turner, who held the same title at RCA Solid State, will head the combined operation, which will be called GE/RCA Solid State Division. He will report to James Dykes, who had headed GE Semiconductor Business Division and has other responsibilities within GE. The new combination consists of a Microelectronics Center at Research Triangle Park, N. C., and GE/RCA Commercial Solid State, in Somerville, N. J. RCA's Herbert Criscito will head up the combined marketing effort, while John Herman, another RCA executive, will be in charge of the Microelectronics Center.

FEDERMAN TAKES THE REINS AT SIA

The Semiconductor Industry Association has a new chairman: Irwin Federman, president of Monolithic Memories Inc., succeeds Gary L. Tooker of Motorola Inc., who is also surrendering his seat on the group's board of directors. James A. Norling, general manager of Motorola's semiconductor operation, who will assume Tooker's chair, joins Wilfred J. Corrigan, chairman of LSI Logic Corp., and Robert Palmer, vice president of Digital Equipment Corp., as newly appointed directors.

WESTERN DIGITAL TO BUY PARADISE

Western Digital Corp. is acquiring Paradise Systems Inc., which produces video controller chips and boards for IBM Corp. Personal Computers and compatibles. Paradise, South San Francisco, Calif., will continue under current management and operate as a wholly owned subsidiary. The acquisition expands Western Digital's product lines, and also brings with it a rare bonus in the chip business: Paradise has a positive book-to-bill ratio. Billings are about $25 million a year, a spokesman says, and bookings are now about $36 million for the coming year.

ENCORE WILL BUILD DARPA MACHINE

Encore Computer Corp., Marlboro, Mass., will build a massively parallel computer system capable of executing 1 billion instructions/s. The company was chosen by the Defense Advanced Research Projects Agency for a three-year, $10.7 million contract as part of the agency's Strategic Computing program. The prototype machine will use Encore's Multimax shared-memory multiprocessor systems as basic building blocks along with hierarchical-cache-memory concepts.

EUROPE EYES HIKE IN VCR PARTS DUTY

The European Association of Consumer Electronics Manufacturers is trying to persuade the Brussels-based European Community to raise import duties for video cassette recorder parts imported from the Far East. The measure, which would raise the rate from 5.8% to 14%, is to eliminate what the group calls an unfair competitive advantage such parts have over fully assembled VCRs, which are subject to a 14% import duty.

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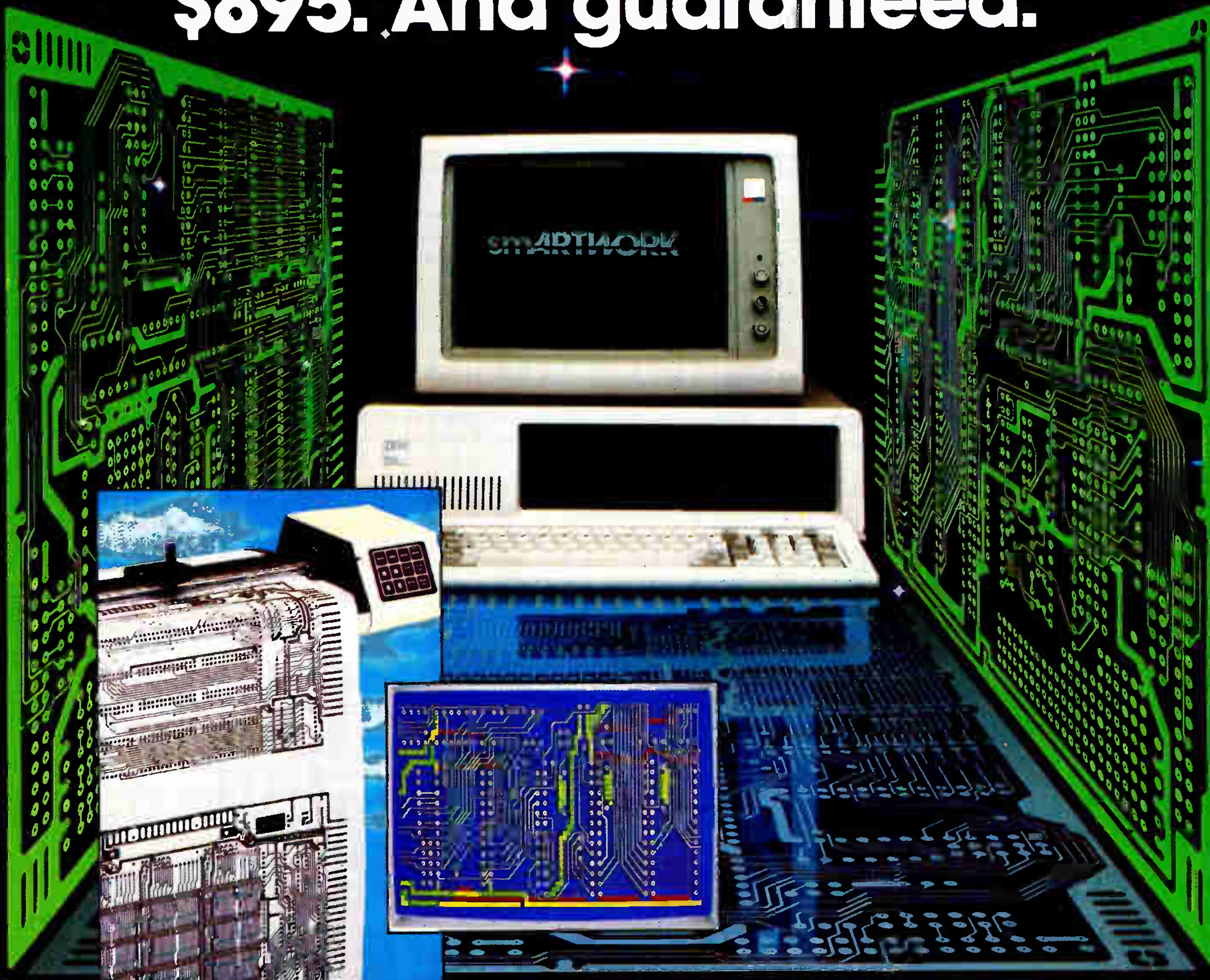

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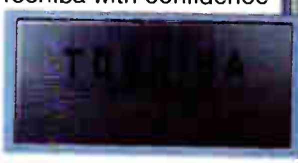

TLC-363

TLC-402

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Input Voltage		0≤VIN≤VDD	VSS≤VIN≤VDD
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